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Improving High-κ Gate Dielectric Properties by High-Pressure Water Vapor Annealing

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High-pressure water vapor annealing has been found to improve the electrical properties of high-κ gate oxides. A vapor-annealing time of less than 60 min was effective in decreasing leakage current density and increasing capacitance density. This improvement is related to the active species in the water vapor which can react with unsaturated bonds in the bulk oxide film and dangling bonds at the film interface. However, the electrical properties did not improve after longer annealing periods. Optimizing the annealing conditions is essential for obtaining high quality high-κ films. [DOI: 10.1143/JJAP.45.L120]

KEYWORDS: high-pressure water vapor annealing, high-κ gate oxides, low temperature annealing

Extensive studies of alternative high-κ gate oxides to replace SiO_2 gate dielectrics have been undertaken.[1–3] In addition, much attention has been focused on improving the quality of high-κ gate oxides for ultra-large scale integration (ULSI) applications. High-pressure hydrogen and deuterium anneals have been reported to be effective in improving high-κ film interface quality.[4,5] The annealing temperature in these studies was 450°C. A previous study has shown that the defective bonds in high-κ films are distributed across the film, unlike those in SiO_2 gate oxide.[6] The electrical and reliability characteristics of thin-film gate dielectrics are sensitive to the concentration of hydrogen-related species in both the bulk oxide and oxide interface. Hydrogen profiles of high-κ gate oxides obtained from nuclear resonant reaction profiling are about one magnitude higher than those of silicon dioxide or oxynitride films.[6] Moreover, the rigid metal silicate bonds in high-κ films make it more difficult to repair all the defective bonds by annealing, compared with SiO_2 films. A method for decreasing defective bonds in high-κ films is, therefore, important, and was the focus of this study. Previously, water vapor annealing was reported as an effective method for improving SiO_2 film quality.[7,8] This process has the advantages of low processing temperature, simplicity, and compatibility with ULSI processes. We found that high-pressure vapor annealing is effective in improving high-κ gate oxide qualities.

High-κ hafnium silicate ($HfSi_xO_y$) films with thickness of 4 and 9 nm were deposited using a polyatomic layer CVD (PL-CVD) on RCA cleaned 8-in. p-type (100) wafers. For the PL-CVD, two types of precursors were used for silicate film depositions. Tetrakis (1-methoxy-2-methyl-2-propoxy)-hafnium [Hf(MMP)$_4$] was the precursor for hafnium, and tetrakis (1-methoxy-2-methyl-2-propoxy)-silicon [(Si(MMP)$_4$)] was the precursor for silicon. A more detailed description of high-κ deposition was given previously.[9,10] After the deposition of the high-κ films, high-pressure water vapor annealing was performed at 260°C and 1.3 MPa steam pressure for different durations. Temperature and pressure for the annealings were previously optimized. After the vapor annealing treatment, MOS capacitors with an aluminum electrode were fabricated for the electrical measurements. The electrical characterization of the deposited gate dielectrics was performed by current–voltage (I–V) and capacitance–voltage (C–V) measurements. An Agilent 4284A impedance analyzer was used for C–V analysis and the I–V characterization was performed using a Keithley 237 parameter analyzer. High-temperature I–V measurements were measured between 298 and 423 K at 30 K intervals.

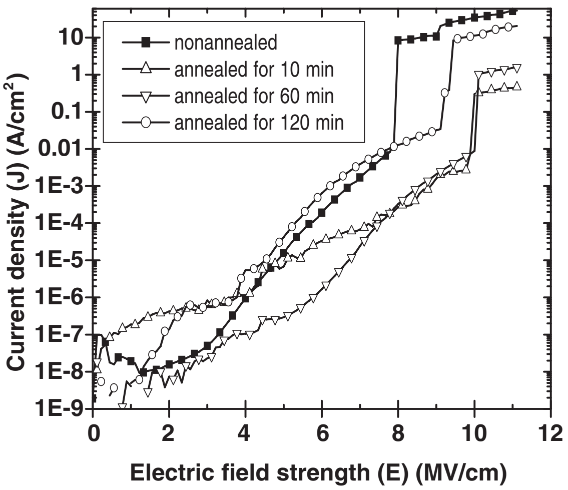

Fig. 1. I–V of $HfSi_xO_y$ films before and after H_2O vapor annealing.

We found that the electrical properties of high-κ films were improved by a short H_2O vapor annealing. Figure 1 shows the changes in leakage current density (J) as a function of electric field strength (E) before and after vapor annealing. The measurements were obtained from many capacitors. One order of magnitude lower leakage current density and a higher breakdown field were observed in the sample annealed at 60 min, compared with the nonannealed sample. The improvement was dominant at high electric field strength. However, current densities increased when the films were annealed longer than 60 min.

High-temperature leakage current measurements indicate that $HfSi_xO_y$ films before and after H_2O vapor annealing have different current transport mechanisms. Figure 2(a) shows the high-temperature J–E results measured at 298–423 K for nonannealed $HfSi_xO_y$ films. The leakage current at a low field ($E < 1.8$ MV/cm) does not depend on temperature, indicating that the direct tunneling mechanism predominates. The current transport of $HfSi_xO_y$ films at a

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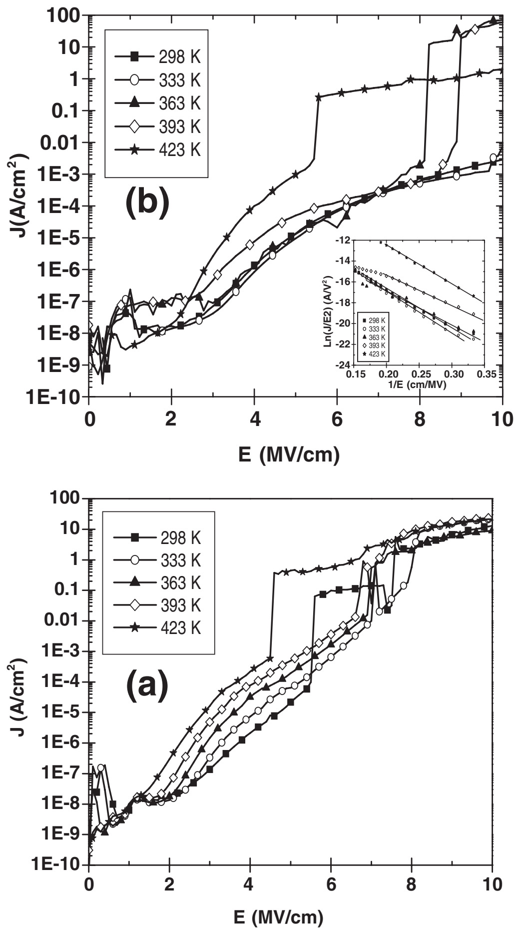

Fig. 2. *I–V* results of samples (a) before and (b) after H_2O vapor annealing, measured at different temperatures. The inset in (b) shows the FN plots of $HfSi_xO_y$ films after H_2O vapor annealing measured at different temperatures.

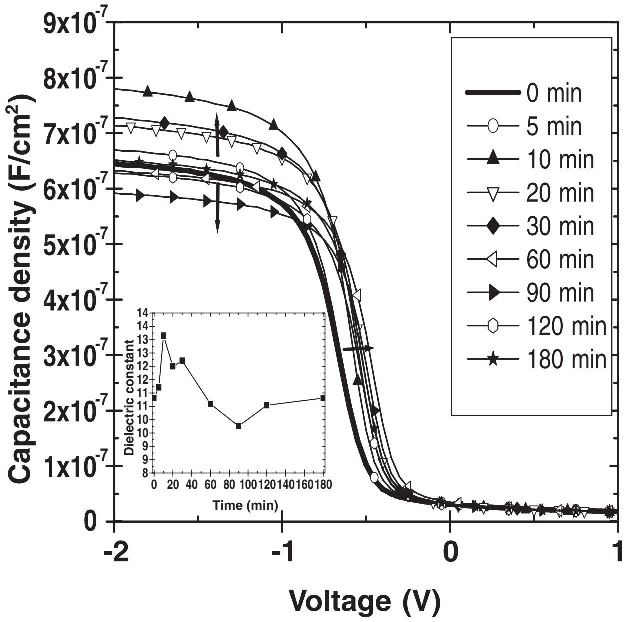

Fig. 3. *C–V* of $HfSi_xO_y$ films before and after H_2O vapor annealing for different times. The inset shows dielectric constants of $HfSi_xO_y$ films for different annealing times.

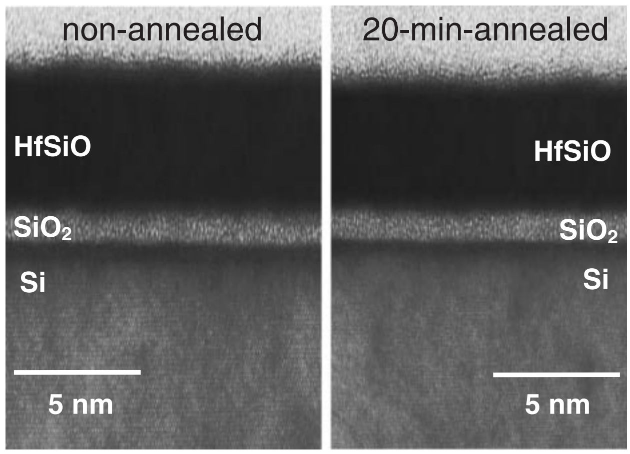

Fig. 4. TEM images of $HfSi_xO_y$ films before and after 20 min H_2O vapor annealing.

medium field (1.8 – 5 MV/cm) depends strongly on temperature, but the dependency on gate current seems to decrease when the gate voltage exceeds 5 V. These results are consistent with the Poole–Frenkel (PF) conduction mechanism, or the trapped assisted tunneling model, as the current transport mechanism in the case of non-annealed $HfSi_xO_y$ gate oxides. In contrast, the leakage current of H_2O vapor-annealed $HfSi_xO_y$ films is less dependent on temperature in all voltage ranges, as shown in Fig. 2(b). However, a large increase in leakage current was observed at 423 K. The reduced dependency of temperature on current suggests that Fowler–Nordheim (FN) tunneling serves as the main charge transport mechanism in the annealed samples. This also indicates that the number of trapped sites decreased after vapor annealing. The FN tunneling plot of vapor-annealed $HfSi_xO_y$ samples is shown in the inset of Fig. 2(b). The m^*/m^{o} was assumed to be 0.1. Therefore, the calculated barrier height (ϕ_{b}) was found to be 1.42 eV.

Figure 3 shows the *C–V* results for samples annealed for different durations. A short ($t < 60$ min) vapor annealing increased capacitance density, but capacitance density decreased when annealing time was longer than 60 min. The increase in capacitance is due to bonding rearrangements in the bulk film. A comparison of dielectric constants at different annealing durations is shown in the inset of Fig. 3; dielectric constant increased when the samples were exposed to vapor annealing of less than 60 min due to film densification, as also observed by TEM. Figure 4 shows TEM images taken from nonannealed and vapor-annealed (20 min) $HfSi_xO_y$ films. The high-κ film thickness decreases after vapor annealing. This result can explain the increase in capacitance density from a short annealing. There is no significant increase in the growth of the interfacial SiO_2 layer after a short annealing. However, a thicker interfacial layer was observed after a long annealing, as confirmed from the decrease in capacitance density. Therefore, less than 60 min of annealing can improve film quality without increasing the interfacial layer growth. The high-pressure water vapor annealing was performed at a lower temperature ($T = 260$°C), as compared with high-pressure oxygen annealing ($T > 450$°C). We found that there is a smaller thermodynamic driven for the interfacial layer growth, as compared with the other high temperature annealing processes.

We observed from the FT-IR results that the numbers of Si–O and Hf–O bonds increase after vapor annealing, as shown in Figs. 5(a) and 5(b). This result also confirms that there were many oxygen-deficient bonds in the high-κ film before the vapor annealing. Active oxygen species in vapor steam can repair these defective Si–O– and Hf–O– bonds and restore the stable bond structure.

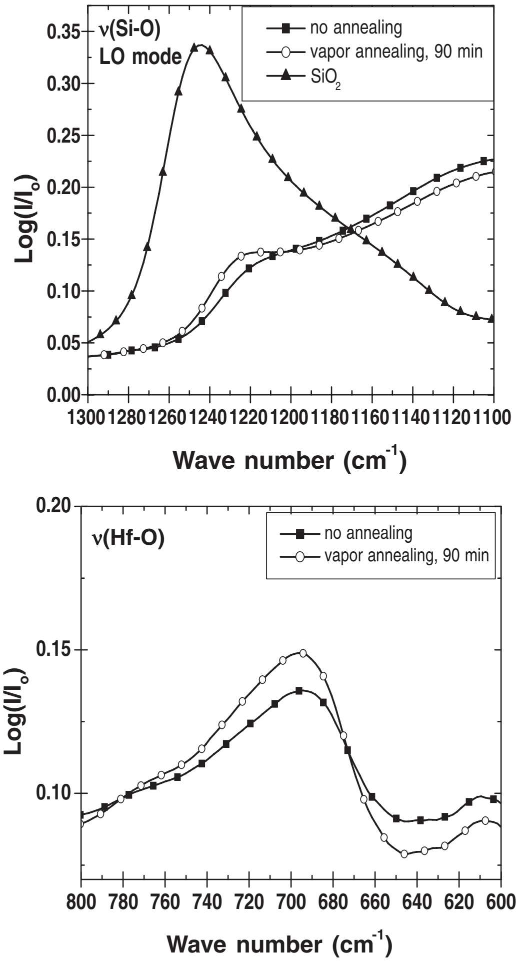

Fig. 5. FT-IR results of (a) Si–O and (b) Hf–O stretching bonds before and after H_2O vapor annealing.

Figure 6 shows a proposed model for explaining the effect of short H_2O vapor annealing on the reduction in the number of defective bonds by hydrogen and oxygen active species. The model is based on the following hypotheses: There are a lot of defective dangling bonds (Si– and Hf–) and electron-trapping bonds (Si–O– and Hf–O–) in the high-κ films before annealing [Fig. 6(a)]. The intrinsic and extrinsic defects in high-κ gate oxides might be responsible for the large shift in their gate threshold voltage and lower carrier mobility as compared with SiO_2 gate oxides.[11] Moreover, the defects in high-κ film are distributed across the film unlike the confined defects at the interface in the case of SiO_2 film.[6] These defective bonds were recovered by active species in the water vapor, as shown in Fig. 6(b). The hydrogen and oxygen active species can decreases density of electronically active defects. The hydrogen active species are small components so they can easily migrate into the oxide film to react with unsaturated sites. This diffusion is important for dangling bond restoration and improving gate oxide qualities. However, longer H_2O vapor annealing can introduce excess –OH bonds and these Si–OH and Hf–OH bonds are the source of charge trapping sites [Fig. 6(c)]. Moreover, the excess annealing results in interfacial layer growth, as confirmed from the *C*–*V* results. Therefore, optimum annealing conditions are necessary.

In conclusion, high-pressure H_2O vapor annealing was found to improve high-κ film qualities. Leakage current is reduced by two orders of magnitude after a short annealing. However, electrical performance deteriorates if annealing time is longer than 60 min. Therefore, optimum annealing conditions are necessary to improve film properties. The active species in high-pressure water vapor annealing decrease the number of defective bonds in the bulk high-κ films at annealing times shorter than 60 min. The current transport of $HfSi_xO_y$ gate oxides depends strongly on temperature, suggesting the PF conduction mechanism, whereas the FN tunneling mechanism was observed in the case of vapor-annealed samples. This low-temperature annealing method is simple and compatible with ULSI processes. Furthermore, it provides an alternative for the low-temperature applications.

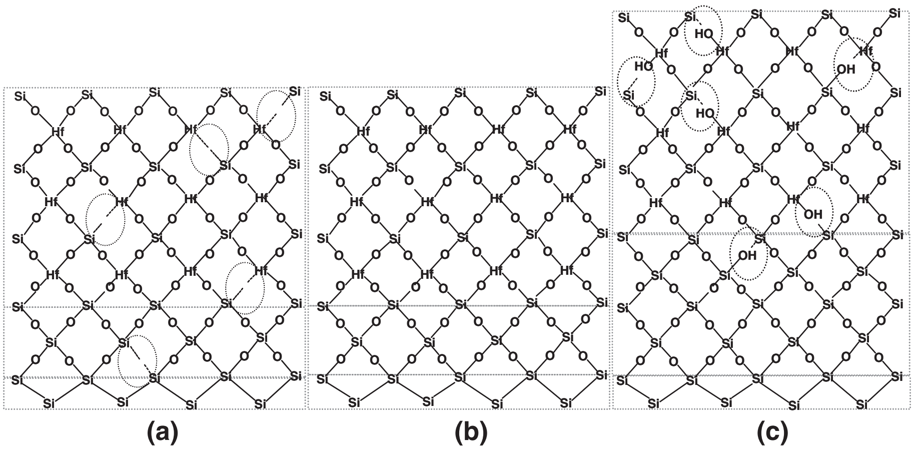

Fig. 6. Model for explaining effects of H_2O vapor annealing for fixing defective bonds in bulk high-κ $HfSi_xO_y$ films. Bond structure (a) before H_2O vapor annealing, (b) after short H_2O vapor annealing, and (c) after more than 60 min of annealing.

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