Polycrystalline Silicon Thin-Film Transistors Fabricated by Rapid Joule Heating Method

Y. Kaneko, N. Andoh, and T. Sameshima

***Abstract*—We report n- and p-channel polycrystalline silicon thin film transistors (poly-Si TFTs) fabricated with a rapid joule heating method. Crystallization of 50-nm-thick silicon films and activation of phosphorus and boron atoms were successfully achieved by rapid heat diffusion via 300-nm-thick SiO_2 intermediate layers from joule heating induced by electrical current flowing in chromium strips. The effective carrier mobility and the threshold voltage were 570 cm^2/Vs and 1.8 V for n-channel TFTs, and 270 cm^2/Vs and −2.8 V for p-channel TFTs, respectively.**

***Index Terms*—Crystallization, defect, joule heating, mobility, polycrystalline silicon (poly-Si), thin film transistors (TFTs), threshold voltage.**

I. Introduction

RAPID thermal annealing is useful for fabrication of polycrystalline silicon thin film transistors (poly-Si TFTs) at low processing temperatures and their application to electrical devices [1]–[7]. Laser crystallization has been widely used for rapid formation of polycrystalline silicon films. Poly-Si TFTs with high carrier mobility have been achieved. However, complicated optical equipment is required in order to deliver the laser beam to samples and to control the distribution of laser beam intensity for laser crystallization. We have recently demonstrated a simple crystallization method using electrical-current-induced joule heating [8], [9] Microsecond order rapid heating is achieved by joule heating caused by electrical current flowing thin metal films.

In this letter, we report fabrication of n- and p-channel poly-Si TFTs. Crystallization of silicon as well as activation of dopant atoms are achieved using the rapid joule heating method. The high carrier mobility demonstrates that t he polycrystalline silicon films fabricated by the joule-heating method have a possibility of device application.

II. Experimental

Fig. 1 shows the fabrication steps of Poly-Si TFTs. Fifty-nanometer-thick undoped amorphous silicon films were formed on glass substrates. Two hundred-nanometer-thick SiO_x islands with lengths of 25 and 100 μm and a width of 70 μm were formed on channel regions of the silicon films as the dopant stopper. Phosphorus and boron atoms were implanted at 10 KeV with a density of 1.3×10^{15} cm^{-2}, respectively. After removing the dopant-stopping-SiO_2 islands,

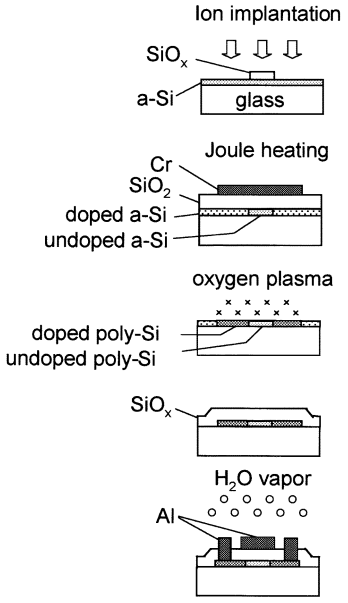

Fig. 1. Schematic fabrication flow of poly-Si TFTs.

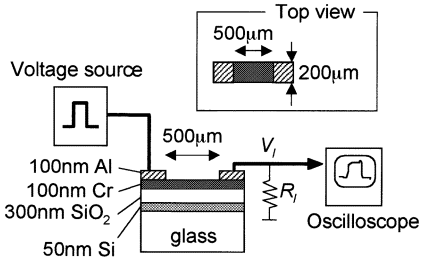

Fig. 2. Schematic apparatus of the rapid joule heating and the cross section of the layered structure of samples. 5-μs-pulsed voltage was applied to 100-nm-thick Cr strip with a length of 500 μm and a width of 200 μm.

crystallization and dopant activation were simultaneously carried out with the joule heating method as shown in Fig. 2. Three hundred-nanometer-thick SiO_2 films were formed on the silicon films. 100-nm-thick chromium films were subsequently formed on the SiO_2 films. Chromium strips with a width of 200 μm and a length of 500 μm were defined above the channel regions. The resistance of the chromium strips was 65 Ω. Aluminum electrodes were formed at the edges of the chromium strips to apply electrical voltages. 5-μs-pulsed voltages were applied to the samples, as shown in Fig. 2. The electrical current was measured as a voltage at a load resistance connected between the sample and ground using a digital oscilloscope in order to obtain the joule heating energy density per unit area. The joule heat generated at the chromium films

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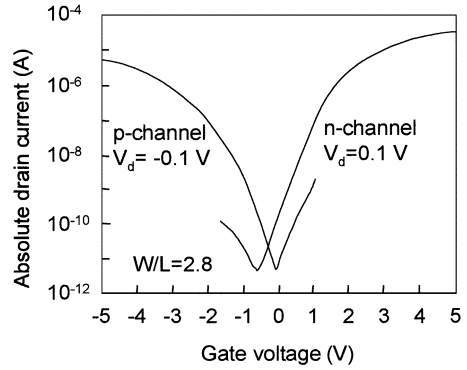

Fig. 3. Transfer characteristics of n- and p-channel poly-Si TFTs with a channel length of 25 μm and a channel width of 70 μm fabricated at joule heating energy densities at 0.75 and 0.74 $\mathrm{J/cm^2}$, respectively.

diffuses into the underlying layer and the silicon film are heated by heat flow through the intermediate SiO_2 layer. The silicon channel regions and source drain regions below the chromium strips were successfully crystallized with no substrate heating. Raman scattering spectra and TEM observation revealed that silicon films were crystallized at a joule heating energy density above 0.58 $\mathrm{J/cm^2}$, the crystallization threshold, caused by 115-V voltage pulse application [8]. The average grain size was about 100 nm at a joule heating energy density of 0.74 $\mathrm{J/cm^2}$. The dopant atoms in the source and drain regions below the chromium strips were also activated. The electrical conductivity became 320 S/cm for phosphorus doping and 280 S/cm for boron doping for joule heating energy density above 0.65 $\mathrm{J/cm^2}$. After removing the SiO_2 layers and the Cr strips, 13.56 MHz-remote-type-oxygen plasma at 100 W, 130 Pa and 250 °C for 30 min was applied to defect reduction in poly Si films [10], [11]. Silicon islands were then defined. SiO_x films 130–150-nm-thick were then formed as the gate insulator by thermal evaporation of SiO powders in the oxygen radical atmosphere at room temperature [12]. Contact holes were opened and then Al gate, source and drain electrodes were formed. After fabrication of the TFT structure, TFTs were heated at 200 °C with 1.3×10^6 Pa $-$ H_2O vapor for 3 h for improvement of SiO_x properties [13]–[16]. Measurements of capacitance response with the gate voltage with a frequency of 1 MHz for Al gate metal-oxide-semiconductor (MOS) capacitors with the SiO_x layer determined that the specific dielectric constant of the SiO_x layer, the densities of interface traps and fixed oxide charges were 4.9, 2.0×10^{10} $\mathrm{cm^{-2}eV^{-1}}$, and 3.4×10^{10} $\mathrm{cm^{-2}}$ after the H_2O vapor heat the treatment, respectively.

III. Results and Discussion

Fig. 3 shows the transfer characteristics of the n- and p-channel poly-Si TFTs with a channel length of 25 μm and a channel width of 70 μm fabricated at joule heating energy densities at 0.75 and 0.74 $\mathrm{J/cm^2}$, respectively. Sharp increase in the drain current with low gate voltage application was observed for the both TFTs. Fig. 4 shows the effective carrier mobility (a) and the threshold voltage (b) obtained by linear relation of the drain current with the gate voltage for TFTs fabricated at the joule heating energy density from 0.60 to 0.78 $\mathrm{J/cm^2}$. The effective

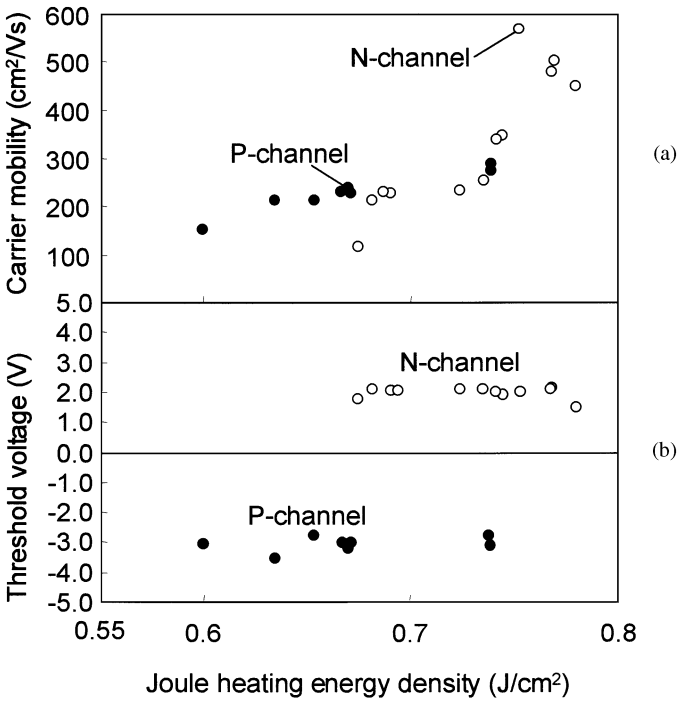

Fig. 4. Effective carrier mobility (a) and the threshold voltage (b) as functions of the joule heating energy density. Open circles represent the carrier mobility and carrier density for n-channel TFTs and solid circles represent them for p-channel TFTs.

carrier mobility increased from 115 to 570 $\mathrm{cm^2/Vs}$ as the joule heating energy density increased from 0.67 to 0.75 $\mathrm{J/cm^2}$ for n-channel TFTs. It increased from 147 to 270 $\mathrm{cm^2/Vs}$ as the joule heating energy density increased from 0.60 to 0.74 $\mathrm{J/cm^2}$ for p-channel TFTs. The high carrier mobility means that silicon films had the high crystalline volume ratio. Moreover there is a possibility of mobility enhancement especially in hole mobility caused by tensile stress [16]. Our previous study revealed that the silicon films crystallized by the present joule heating method had a high tensile stress in the silicon films $\sim 6 \times 10^8$ Pa due to difference in thermal expansion coefficient between silicon and glass substrate [9]. The threshold voltage distributed between 1.8 and 2.2 V for n-channel TFTs, and it distributed between -3.5 and -2.8 V for p-channel TFTs as shown in Fig. 4(b). Almost same characteristics on the carrier mobility and threshold voltage were obtained for TFTs with the channel length of 100 μm.

In order to estimate the density of defect states in polycrystalline silicon films, transfer characteristics shown in Fig. 3 were analyzed using a numerical calculation program constructed with the finite-element method combined with statistical thermodynamical conditions with localized defect states at SiO_2/Si interfaces and silicon films [17], [18]. The total density of defect states including acceptor and donor type defects trapping electrons and holes, respectively, was estimated as 1.3×10^{12} $\mathrm{cm^{-2}}$.

The results of Figs. 3 and 4 demonstrated that the present rapid joule heating can be applied to crystallization of silicon films and activation of dopant atoms in TFT fabrication steps. Fabrication of TFTs with a high carrier mobility and a low threshold voltage is possible at low processing temperature.

However, defects remained in polycrystalline silicon probably caused high leakage currents due to carrier recombination at the junctions of channel/doped regions. The density of defect states should be further reduced.

IV. Summary

The rapid joule heating method using 65-Ω-chromium strips was applied for crystallization of 50-nm-thick silicon films and activation of dopant atoms for fabrication of polycrystalline silicon thin film transistors (poly-Si TFTs). The joule heating at $0.6 \sim 0.78\ \mathrm{J/cm^2}$ successfully formed undoped crystalline silicon channel regions and doped source and drain regions. Activation of dopant atoms was also achieved. Defect reduction treatment of 13.56 MHz-oxygen plasma at 100 W, 130 Pa at 250 °C for 30 min was used after crystallization of silicon films. Heat treatment at 200 °C with 1.3×10^6 – Pa – H_2O vapor for 3 h were also applied after TFT fabrication in order to improve electrical properties of SiO_x gate insulator. N-channel TFTs had an effective carrier mobility of 570 $\mathrm{cm^2/Vs}$ and a low threshold voltage of 1.8 V at a joule heating energy density of $0.75\ \mathrm{J/cm^2}$. P-channel TFTs had an effective carrier mobility of 270 $\mathrm{cm^2/Vs}$ and a low threshold voltage of -2.8 V at $0.74\ \mathrm{J/cm^2}$. Those results show that the polycrystalline silicon films formed by the present joule heating have a good enough quality to TFT operation.

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