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# Rapid Joule Heating of Metal Films Used to Fabricate Polycrystalline Silicon Thin Film Transistors

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We report fabrication of p-channel polycrystalline silicon thin film transistors (poly-Si TFTs) at a low temperature using a rapid crystallization joule heating method. Fifty-nm-thick silicon films were crystallized via 300-nm-thick $SiO_2$ intermediate layers by heat diffusion from joule heating induced by electrical current flowing in chromium strips. The maximum grain size was about 100 nm. Oxygen plasma of 13.56 MHz at 100 W, 130 Pa and 250°C was applied for 5 min for defect reduction in the polycrystalline silicon films. Heat treatment at 200°C with $1.3 \times 10^6$-Pa-$H_2O$ vapor was applied for 3 h to improve electrical properties of $SiO_x$ gate insulator. TFTs had a high carrier mobility of 204 $cm^2/V{\cdot}s$ and a low threshold voltage of $-2.1$ V. [DOI: 10.1143/JJAP.41.L913]

KEYWORDS: joule heating, crystallization, poly-Si, TFT, defect, mobility

Rapid annealing is attractive for formation of polycrystalline silicon (poly-Si) films at low processing temperatures and the application of poly-Si to the fabrication of electrical devices such as thin film transistors (TFTs).[1–5] Laser crystallization has been widely used for rapid formation of polycrystalline silicon films. Poly-Si TFTs with good performance have been reported. For laser crystallization, optical equipment is required in order to deliver the laser beam to samples and to control the distribution of laser beam intensity. We have recently demonstrated a simple crystallization method using electrical-current-induced joule heating.[6,7] Silicon films have been rapidly heated and crystallized through heat diffusion from thin metal films heated by electrical-current-induced joule heating.

In this paper, we report fabrication of p-channel polycrystalline silicon thin film transistors (poly-Si TFTs) using the rapid joule heating method. A high carrier mobility of 204 $cm^2/V{\cdot}s$ and a low threshold voltage of $-2.1$ V demonstrate that the polycrystalline silicon films fabricated by the present method are suitable for device application.

Figure 1(a) shows a schematic apparatus of the present joule heating for crystallization of silicon films. Undoped amorphous silicon films with a thickness of 50 nm were formed by low pressure chemical vapor deposition (CVD) methods on glass substrates. 300-nm-thick $SiO_2$ films were formed on the silicon films by sputtering. 100-nm-thick chromium films were subsequently formed on the $SiO_2$ films. Chromium strips with a width of 200 $\mu$m were defined by etching. Aluminum electrodes with a gap of 500 $\mu$m were also formed on the chromium strips to apply electrical voltages. The resistance of the chromium strips was 70 $\Omega$. Pulsed voltages with a duration of 5 $\mu$s were applied to the samples, as shown in Fig. 1(a). The electrical current was measured as a voltage $V_l$ at the 2.2-$\Omega$-load resistances $R_l$ connected between the sample and ground using a digital oscilloscope in order to obtain the joule heating intensity. The joule heating intensity per unit area $P(t)$ is given as

$$P(t) = \frac{\left(V_0 - V_l\left(1 + \dfrac{R_s}{R_l}\right)\right) V_l}{R_l S}, \qquad (1)$$

where $V_0$ is the applied voltage, $R_s$ is the series resistance, 10 $\Omega$ of the circuit and $S$ is the area of the chromium strips. The joule heat generated in the chromium films diffuses into the underlying layers and the silicon films are heated by heat flow through the intermediate $SiO_2$ layer. A heat intensity of 0.7-MW/$cm^2$ was generated in the Cr strips at an applied voltage of above 140 V. Figure 1(b) shows the fabrication steps of TFTs. 50-nm-thick undoped amorphous silicon films were crystallized by joule heating at 5-$\mu$s-pulsed voltage of 140 V applied to the Cr strips, as shown in Fig. 1(a). After removing the Cr strips and the $SiO_2$ intermediate layers, 20-nm-thick $SiO_x$ and Al strips with a length of 25 $\mu$m

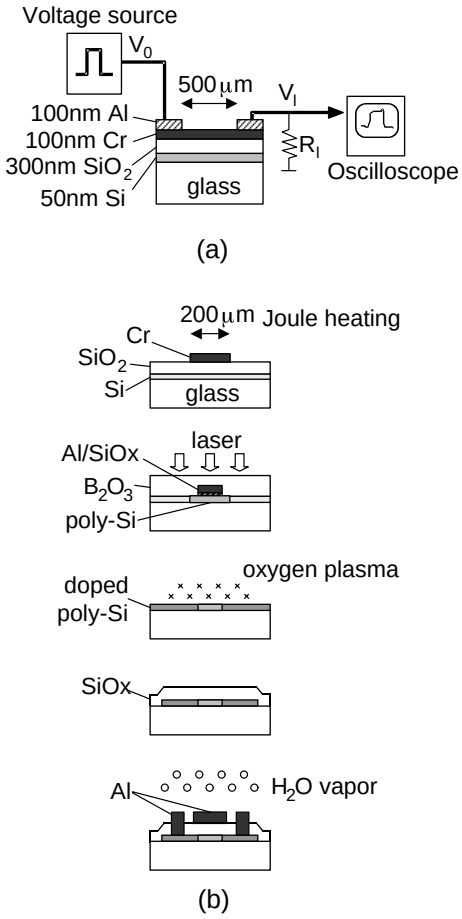


Fig. 1. Schematic apparatus of the rapid joule heating of metal films and the cross section of the layered structure of samples (a). 5-$\mu$s-pulsed voltage was applied to 100-nm-thick Cr strip with a length of 500 $\mu$m and a width of 200 $\mu$m. (b) is schematic fabrication flow of poly-Si TFTs.

were formed on the channel regions of the polycrystallized silicon films. A dopant source of 150-nm-thick $B_2O_3$ layer was formed on the sample surface by spin coating of an organic liquid which consisted of an organic binder and $B_2O_3$ molecules. The samples were irradiated with XeCl excimer laser pulses at 420 mJ/cm$^2$. Boron atoms were diffused into the silicon films and doped silicon films were formed. A conductivity of 22 S/cm was achieved in the doped silicon. Hall effect current measurements revealed a carrier concentration of $4 \times 10^{19}$ cm$^{-3}$. In contrast, the silicon region below the Al layer was not heated by laser irradiation due to reflectance of laser light. After removing the dopant films and Al/$SiO_x$ films, 13.56 MHz oxygen plasma at 100 W, 130 Pa at 250°C was applied for 5 min for defect reduction in the polycrystalline silicon films.[8] After silicon island formation, 280-nm-thick $SiO_x$ films were formed as the gate insulator by thermal evaporation of SiO powders at room temperature.[9] Contact holes were opened and then Al gate, source and drain electrodes were formed. After formation of the TFT structure, TFTs were heated at 200°C with $1.3 \times 10^6$ Pa-$H_2O$ vapor for 3 h for oxidation of $SiO_x$.[10,11] C–V measurement determined the dielectric constant of $SiO_x$ and the density of defect states.

The silicon layers were rapidly heated and crystallized by heat diffusion from the hot chromium layers at the applied voltage of 140 V. Figure 2 shows a micrograph of the bright field image of the transmission electron microscope (TEM) plane view for silicon films crystallized by the present method at 140 V. The silicon region underlying the Cr strips was completely crystallized. Fine crystalline grains with sizes ranging between 50 and 100 nm were closely formed.

Figure 3 shows capacitance responses with the gate voltage with a frequency of 1 MHz for Al gate metal-oxide-semiconductor (MOS) capacitors with the present $SiO_x$ as-fabricated and annealed at 200°C with $1.3 \times 10^6$ Pa $H_2O$ vapor for 3 h. A sharp capacitance transition was observed. From the curve of capacitance versus gate voltage, the specific dielectric constant of the $SiO_x$ layer, the densities of interface traps and fixed oxide charges were estimated to be 16.8, $2.0 \times 10^{10}$ cm$^{-2}$·eV$^{-1}$ and $7.1 \times 10^{11}$ cm$^{-2}$, respectively, for as fabricated MOS capacitors. The high-pressure $H_2O$ vapor heat treatment oxidized $SiO_x$ layers so that the maximum oxide capacitance decreased as shown in Fig. 3. The specific dielectric constant of the $SiO_x$ layer, the densities of interface traps and fixed oxide charges were estimated to be 4.9, $2.0 \times 10^{10}$ cm$^{-2}$·eV$^{-1}$ and $3.4 \times 10^{10}$ cm$^{-2}$, respectively, after the $H_2O$ vapor heat treatment. The density of the fixed oxide charges was markedly reduced because of the reduction of silicon dangling bonds in $SiO_x$ films.

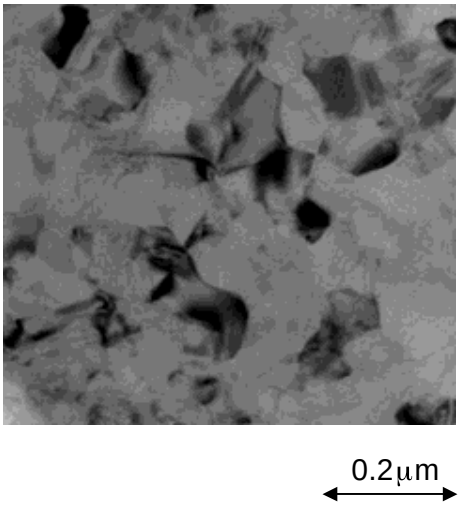


Fig. 2. Micrograph of the bright field image of transmission electron microscope (TEM) plane view for 50-nm-thick silicon films crystallized by the rapid joule heating of metal films at 140 V.

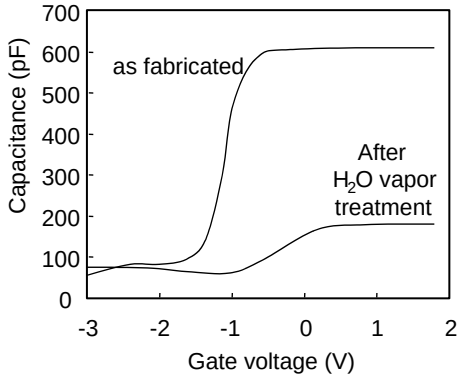


Fig. 3. C–V characteristics at 1 MHz for Al gate metal-oxide-semiconductor (MOS) capacitors with $SiO_x$ as fabricated and treated with $1.3 \times 10^6$-Pa-$H_2O$ vapor heating at 200°C for 3 h. The area of gate Al metal was $5.5 \times 10^{-3}$ cm$^2$.

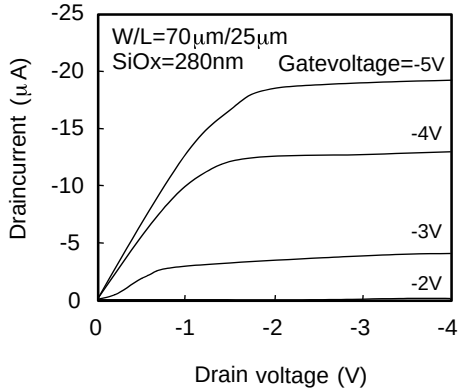


Fig. 4. Output characteristics of p-channel poly-Si TFTs with a channel length of 25 $\mu$m and a channel width of 70 $\mu$m.

Figure 4 shows the output ($I_d$-$V_d$) characteristics of the p-channel poly-Si TFT with a channel length of 25 $\mu$m and a channel width of 70 $\mu$m. It shows good ohmic characteristics and a high drain current. Figure 5 shows the transfer characteristic of the TFTs. The threshold voltage was −2.1 V. The maximum effective carrier mobility in the linear region was 204 cm$^2$/V·s. The minimum subthreshold slope was 0.25 V/decade. The results of Figs. 4 and 5 indicate that the polycrystalline silicon films formed by the present joule heating method have sufficient quality for TFT operation.

In order to estimate the density of defect states in polycrystalline silicon films, transfer characteristics were analyzed using a numerical calculation program, which was constructed with the finite-element method combined with statistical thermodynamical conditions with defect states localized at $SiO_2$/Si interfaces as well as silicon films.[12,13] We introduced the deep-level defect states localized at the mid gap, which had a Gaussian-type energy distribution. Tail-

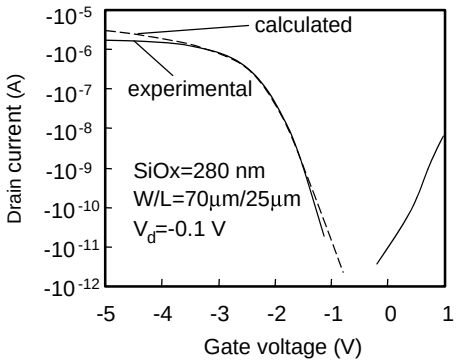


Fig. 5. Transfer characteristics of p-channel poly-Si TFTs. The solid curve is experimental drain current and the dashed curve is calculated drain current.

state-type defect states were also introduced. The density exponentially decreased from the valence band as well as the conduction band edges to the deep energy level in the band gap. The defect states were placed uniformly in the silicon films. The density of defect states at $SiO_2$/Si interfaces was determined by C–V measurements of MOS capacitors to be $2 \times 10^{10}\,\mathrm{cm}^{-2}\cdot\mathrm{eV}^{-1}$. The best agreement of calculated transfer characteristics to experimental ones resulted in the density of defect states. The calculated drain current is shown by the dashed curve in Fig. 5. The calculation suggested that the silicon channel of the present TFTs had duplicate tail states with widths of 0.04 eV and 0.26 eV. The densities of unoccupied tail states in the flat band condition was $3.8 \times 10^{11}\,\mathrm{cm}^{-2}$ for the width of 0.04 eV and $1.9 \times 10^{11}\,\mathrm{cm}^{-2}$ for 0.26 eV. The density of unoccupied states at mid gap was $2.0 \times 10^{11}\,\mathrm{cm}^{-2}\cdot\mathrm{eV}^{-1}$. The low density of defect states enabled a marked increase in the hole carrier density with a low gate voltage application.

In summary, the rapid heating properties of joule heating induced by electrical current flowing in chromium strips were employed in order to crystallize 50-nm-thick silicon films for fabrication of poly-Si TFTs. The application of pulsed voltage at 140 V for 5 $\mu$s caused a rapid crystallization of the silicon films with a maximum grain size of 100 nm via 300-nm-thick $SiO_2$ intermediate layers. P-channel poly-Si TFTs were fabricated by the formation of a boron-doped source drain region using the laser-doing method. Defect reduction treatment of 13.56 MHz-oxygen plasma at 100 W, 130 Pa at 250°C was applied for 5 min to the crystallized silicon films. Heat treatment at 200°C with $1.3 \times 10^6$-Pa-$H_2O$ vapor was for 3 h also applied after TFT fabrication in order to improve electrical properties of $SiO_x$ gate insulator. Poly-Si TFTs had high carrier mobility of $204\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ and low threshold voltage of $-2.1$ V. The numerical calculation suggested that tail-type defect were dominant in the silicon films. The densities of unoccupied tail states in the flat band condition are $3.8 \times 10^{11}\,\mathrm{cm}^{-2}$ for a width of 0.04 eV and $1.9 \times 10^{11}\,\mathrm{cm}^{-2}$ for 0.26 eV. The results indicate that the polycrystalline silicon films formed by the present joule heating method have sufficient good quality for TFT operation.

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