Jpn. J. Appl. Phys. Vol. 41 (2002) pp. 5513–5516
Part 1, No. 9, September 2002

Crystalline Grain Growth in the Lateral Direction for Silicon Thin Films by Electrical Current-Induced Joule Heating

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(Received November 12, 2001; accepted for publication May 22, 2002)

Large crystalline grain growth was demonstrated for 60-nm-thick silicon films using the electrical-current-induced joule heating method. Tapered electrodes were used in order to ensure distribution of the joule heating intensity in the lateral direction along the surface in silicon strips. Melting of silicon for 17 μs caused by the joule heating resulted in the formation of 4–8-μm-long crystalline grains. The change in the film thickness was at most 6 nm in the crystallized region. There was a tensile stress of 5.6×10^8 Pa in the film. The heat flow simulation demonstrated that the solidification occurred in the lateral direction according to the temperature gradient and that the solid/liquid interface moved in the lateral direction at the velocity of about 1–2 m/s. [DOI: 10.1143/JJAP.41.5513]

KEYWORDS: recrystallization, crystal structure, growth model, computer simulation, semiconducting silicon

1. Introduction

The formation of polycrystalline silicon films on foreign substrates such as glass has been important for device applications such as thin film transistors (TFTs) and solar cells. Many technologies have been reported for the formation of polycrystalline silicon films at low processing temperatures.[1–10] Rapid thermal crystallization methods such as, for example, the laser crystallization or photo-current assisted crystallization methods, have been recently applied to the formation of high-quality polycrystalline silicon films with a large grain size.[11–14] We have also reported a crystallization method involving electrical-current-induced joule heating of silicon films in order to fabricate large crystalline grains in the lateral direction.[15–18] We have demonstrated the possibility of controlling the solidification parameters such as the melt duration and the cooling rate using simple electrical circuits.

In this paper, we propose crystalline grain growth in the lateral direction during the electrical-current-induced joule heating of silicon thin films using tapered electrodes. Temperature distribution in the lateral direction is achieved by spatially controlling the joule heating intensity using tapered electrodes. We discuss the melt-regrowth process from the results of heat flow numerical analysis and observation under a transmission electron microscope (TEM). The change of the film thickness and the film stress are also discussed.

2. Experimental

60 nm-thick amorphous silicon films were prepared on glass substrates by the low-pressure chemical vapor deposition method. Silicon strips with a width of 30 μm were defined. Tapered-shaped Al/Cr double layered electrodes were formed on the silicon strips for voltage application. Cr was used to prevent diffusion of Al atoms into silicon during heating. The edge of the Al/Cr electrode was slanted on the one side so that the length of the gap between the electrodes changed from 142 μm to 98 μm as shown in the inset in Fig. 1. In the longer side of the silicon region, the electrical resistance is high and the electrical current is low. Therefore, the joule heating intensity can be low. On the other hand, high joule heating intensity can be generated in the shorter side of the silicon region because of low electrical resistance. Consequently, the spatial distribution of the joule heating intensity can be realized. A voltage of 90 V was applied to the silicon strip through electrodes and a capacitor of 0.33 μF connected to the silicon strip in parallel as shown in Fig. 1. When a 5-ns-pulsed laser (355 nm) was irradiated to silicon strips in order to melt silicon and reduce the resistance of the silicon strip, the charge accumulated at the capacitance provided electrical current to the silicon strip. The electrical current was measured as the voltage at the load resistance between the sample and ground. We used a TEM (HITACHI H-9000NAR) to observe the distribution of crystalline grains formed in the silicon thin films. TEM observation was carried out after etching of the glass substrate by the ion milling method from the rear surface. We investigated the distribution of film thickness by stylus step measurement. We also measured Raman scattering spectra to investigate the transverse optical phonon states. We estimated the temperature change of silicon caused by time-dependent joule heating using a numerical analysis program in order to investigate the process of melt-regrowth of silicon strips.

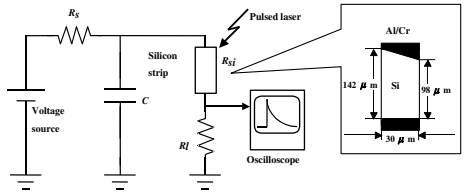

Fig. 1. Equivalent circuit of electrical-current-induced joule heating, which consisted of a voltage source, a series resistance of 10 kΩ and a capacitor of 0.33 μF, the sample and a load resistance of 5 Ω. The inset shows the 60-nm-thick silicon strip and Al/Cr electrodes for voltage application (top view). 5-ns-pulsed 355 nm YAG laser was used for melting silicon.

3. Results and Discussion

Figure 2 shows the change of the electrical current flowing in silicon strips with time. The electrical current was observed for 17 μs. This means that the complete or partial melting of silicon continued for a long time, 17 μs, from the initiation of 5-ns pulsed laser irradiation because of the electrical-current-induced joule heating. The electrical con-

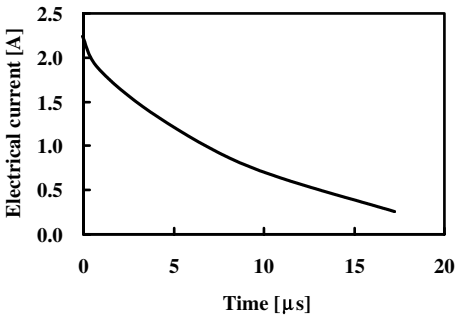

Fig. 2. Change of the electrical current flowing in silicon strips with time when 90 V was applied to the silicon strip as well as the 0.33 μF capacitor.

ductance of the silicon films, $C(t)$, and the average joule heating intensity per unit area, $P(t)$, are experimentally given using the electrical current flowing in silicon strip $I_{Si}(t)$ shown in Fig. 2 as

$$C(t) = \frac{I_{Si}(t)}{V_0 - \frac{1}{C}\int_0^t I_{Si}(t)dt - (R_l + R_c)I_{Si}(t)}, \tag{1}$$

$$P(t) = \frac{I_{Si}(t)^2}{C(t) \cdot S}, \tag{2}$$

where V_0 is the initial applied voltage, C is the capacitance, R_l is the load resistance, R_c is the resistance including that of the metal electrode layers and metal/Si contact and S is the area of the silicon strips. Figure 3 shows changes in the electrical conductance and the average joule heating intensity per unit area in the case of the electrical current flowing in the silicon strip shown in Fig. 2. The electrical conductance of silicon strips had the maximum value of 0.023 S/sq for the first 4.5 μs. This means that the silicon film completely melted within 4.5 μs.[19] The electrical conductance gradually decreased from 4.5 μs to 17 μs. This shows that the solidification of the liquid silicon layer was initiated at 4.5 μs and it completed at 17 μs. The average joule heating intensity monotonically decreased from the high initial value at 4×10^6 W/cm^2. It exponentially decreased with the time constant in the initial stage up to 4.5 μs. Afterwards, the joule heating intensity decreased further due to the reduction of the electrical conductance of the silicon strips because of solidification. The joule heating intensity is lower at the longer side of the silicon strip than the shorter side. Moreover, observation under an optical

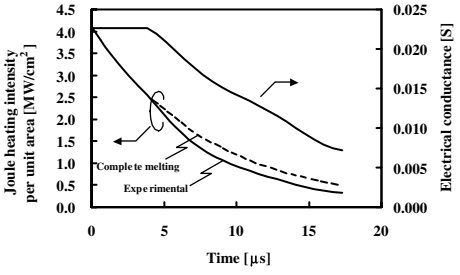

Fig. 3. Changes of the joule heating intensity per unit area and the electrical conductance of silicon strip with time. The dashed carve shows the calculated joule heating intensity as a function of time if silicon strips were completely melted.

microscope revealed that crystallized regions were formed parallel to the silicon strip in the length direction. We therefore infer that the reduction of the electrical conductance of the silicon strip resulted from the solidification proceeding from the longer side to the shorter side of the silicon strip. When the liquid silicon is assumed to maintain a strip shape parallel to the initial silicon strip during solidification, the relation between the electrical conductance $C(t)$ and the position of the liquid silicon region with the longer side $x_l(t)$ and shorter side, $x_s(t)$ in the width direction is expressed as

$$\begin{aligned} C(t) &= A \cdot \int_{x_l(t)}^{x_s(t)} \frac{\sigma \cdot d}{L(x)} dx \\ &= \frac{A \cdot \sigma \cdot d \cdot W}{L_s - L_l} \ln \frac{(L_s - L_l)x_s(t) + L_l W}{(L_s - L_l)x_l(t) + L_l W}, \end{aligned} \tag{3}$$

where the x-axis is positioned along the width direction and $x = 0$ and W are at the edges of longer and shorter side, respectively, W is the width of the strip of 30 μm, $L(x)$ is the length at x of the silicon strip, L_l is the length of the strip on the longer side, 142 μm, L_s is the length of the strip on the shorter side, 98 μm, d is the film thickness of 60 nm, σ is the electrical conductivity of the liquid silicon, which is assumed to be independent of temperature, and A is the experimental factor, which was given by variations of the liquid silicon area in the length direction of the strip or the film thickness. We assumed that the electrical conductivity of solid silicon was negligible compared with the electrical conductivity of the liquid silicon σ. The experimental result for the electrical conductance shown in Fig. 3 reveals that $x_l(t) = 0$ and $x_s(t) = W$ until 4.5 μs because of the complete melting of the strip. The electrical conductance in the complete melting case is described as

$$C_0 = \frac{A \cdot \sigma \cdot d \cdot W}{L_s - L_l} \ln \frac{L_s}{L_l}, \tag{4}$$

We determined the A value from the experimental conductance and eq. (4). The result of Fig. 3 shows that the width of the liquid silicon decreased due to solidification after 4.5 μs. In order to estimate the melt-solidification process, we calculated the temperature change of the silicon strip caused by the time-dependent joule heating intensity. For calculation of temperature, the density of joule heating intensity per unit volume, $Q(x,t)$, at a point x and time t is given using the electrical conductance $C(t)$ and average joule heating intensity per unit area $P(t)$ as,

$$Q(x,t) = \frac{\sigma \cdot I_{Si}(t)^2}{L(x)^2 \cdot C(t)^2} = \frac{\sigma \cdot S \cdot P(t)}{L(x)^2 \cdot C(t)}, \tag{5}$$

From eqs (2)–(5), $Q(x,t)$ is therefore described as

$$Q(x,t) = \frac{W^2(L_s^2 - L_l^2)P(t)}{2d((L_s - L_l)x + L_l W)^2 \ln \frac{(L_s - L_l)x_s(t) + L_l W}{(L_s - L_l)x_l(t) + L_l W}} \cdot \frac{1}{A}, \tag{6}$$

We calculated the temperature change of the silicon strip by applying a numerical analysis program using the density of joule heating intensity per unit volume $Q(x,t)$ as the heat source. The finite element method was used in this program. The program was constructed two-dimensionally with a

system of heat flow equations derived from a heat-balance condition at each of a set of points along the depth direction and the lateral direction along the width of the silicon strip in order to analyze temperature distribution for a multilayered structure comprising different materials. For the point (i,j), the equation is[19,20]

$$\frac{T_{i,j}^{n+1}-T_{i,j}^{n}}{\Delta t}=\frac{Q_{i,j}}{c_{i,j}\rho_{i,j}}+\frac{1}{\Delta^2}\left(\sum_{l=-1}^{+1}(D_{i+l,j}^{n}(T_{i+l,j}^{n}-T_{i,j}^{n})+\sum_{m=-1}^{+1}(D_{i,j+m}^{n}(T_{i,j+m}^{n}-T_{i,j}^{n})\right), \tag{7}$$

where Δ is the distance from the neighboring lattice point of the finite element, $T_{i,j}^{n}$ is the temperature at time t_n of the point (i,j), $D_{i+l,j}^{i,j}$ is the average thermal diffusivity constant between points (i,j) and $(i+l,j)$, $c_{i,j}$ is the specific heat, $\rho_{i,j}$ is the density of weight and $Q_{i,j}$ is the heating intensity per unit volume at point (i,j). The temperatures of the silicon thin films were determined by the heat balance between the heat supply from the joule heating intensity and heat dissipation into glass substrates. We assumed that silicon melted at 1685 K for every heating case and the temperature was maintained at the melting point until the latent heat energy (1810 J/g)[21] was given to the silicon layer. Until 4.5 μs, temperature was calculated under the condition of complete melting of the silicon strip, as indicated by the experimental results. The density of the joule heating intensity was given for all points of the silicon layer in the finite element system. After 4.5 μs, there was a solid silicon region as well as a liquid silicon region in the silicon strip because of the solidification of silicon. Temperature at time $t+\Delta t$ was calculated using the joule heating intensity, $Q(x,t)$, at the prior time t for all cases of the position and width in the liquid silicon region indicated by $x_l(t)$ and $x_s(t)$, respectively, which satisfied eq. (3). The liquid silicon region was defined as the region in which the temperature was above or equal to the melting temperature. The conductance of liquid silicon and $x_l(t+\Delta t)$ and $x_s(t+\Delta t)$ at $t+\Delta t$ were also obtained. The most probable position and width of liquid silicon for $x_l(t+\Delta t)$ and $x_s(t+\Delta t)$ at $t+\Delta t$ was determined when the calculated conductance of liquid silicon was coincident with the experimental conductance at $t+\Delta t$ shown in Fig. 3. The temperature distribution in the width direction was consequently obtained via these calculation steps. Figure 4 shows the temperature distribution at the silicon surface in the lateral direction from the edge of longer side to the edge of shorter side with different times. The position where temperature decreased below the melting point corresponds to the region of the solid phase, and the position under the temperature is 1685 K corresponds to the region of the liquid phase. The temperature at the edge of longer side first decreased at 4.5 μs below the melting point because of the low joule heating intensity as well as heat diffusion to the periphery of the strip, while the other region was in the liquid phase at the melting point. Afterwards, the solidification proceeded from the edge of longer side towards the edge of shorter side. The solidification velocity, estimated from the velocity of the movement of the liquid–solid interface, was initially 1.2 m/s. It gradually increased to 2.0 m/s. It is interesting that the solidification also occurred from the edge of shorter side 14 μs after the initiation of silicon melting, as shown in Fig. 4. The temperature decreased at the edge of shorter side because of the heat diffusion into the glass substrate in the lateral direction, although the joule heating intensity was high. The results of heat flow calculation consequently showed a decrease of the temperature at the position 6 μm inside the edge of shorter side below the melting point at 17 μs. This means that the solidification was complete 6 μm inside the edge of shorter side 17 μs after the initiation of silicon melting, based on the results of the heat flow simulation. The cooling rate at the leading edge of solidification was high at 1.7×10^{8} K/s at the onset of solidification. It decreased to 6.1×10^{7} K/s at the termination of the solidification as shown by reduction of the temperature gradient in the depth direction associated with heat diffusion into a deeper region. Figure 5 shows a bright-field image obtained from TEM observation at the shorter side. Formation of large crystalline grains was observed in the region over 18 μm from the edge of the shorter side of the silicon strip. In the region, many bend contours were observed, as shown by arrows in Fig. 5. Those clearly indicate that there was growth of crystalline grains with sizes from 4 μm to 8 μm. The heat flow calculation suggests that the crystalline grain growth in the lateral direction occurred during the electrical-current-induced joule heating with the tapered electrodes. The large grains were probably formed according to movement of the solid/liquid front, as shown in Fig. 4. Figure 6 shows the distribution of the film thickness in the crystallized region with large grains near the shorter side measured by stylus step. The film thickness distribution

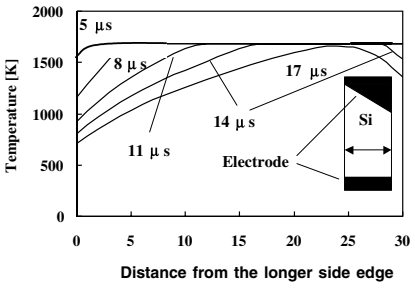

Fig. 4. Temperature distribution at the silicon surface in the lateral direction from the longer silicon side to the shorter silicon with side different times. Inset presents schematic illustration of sample with tapered- electrodes.

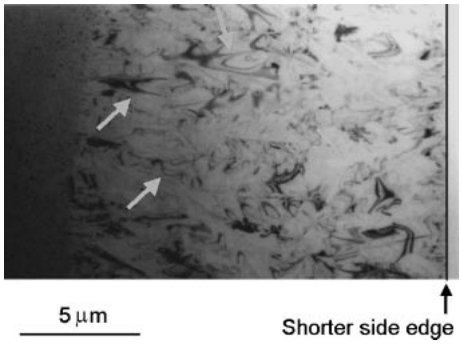

Fig. 5. Bright-field image of silicon films crystallized by the joule heating method with application of 90 V observed by a transmission electron microscope.

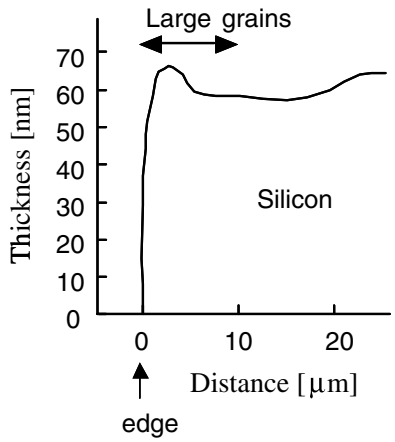

Fig. 6. Film thickness distribution near the shorter sides of silicon strips determined by stylus step measurement.

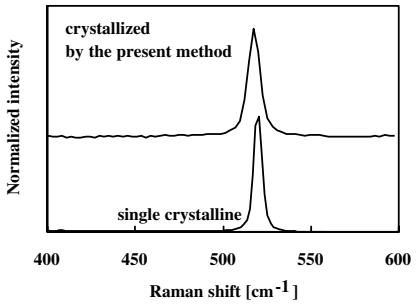

Fig. 7. Raman scattering spectra of region with large crystalline grains formed by the electrical-current-induced joule heating method and single crystalline silicon. Upper line indicates the spectra of silicon films crystallized by the joule heating method and lower one indicates that of single crystalline silicon.

was from 66 nm to 58 nm. The film thickness changed negligibly compared with the initial amorphous silicon thickness. This means that silicon atoms in the liquid state did not move much on the quartz substrates. Although the measurement of the electrical conductance indicated that the silicon strip completely melted in the initial 4.5 μs, there was tight bonding between the silicon and substrate surface during the melt-regrowth process. Figure 7 shows the Raman scattering spectrum of crystallized silicon film with large grains and that of single crystalline silicon. In the films crystallized by the present method, the sharp crystalline transverse optical (TO) phonon peak was observed around 517.4 cm^{-1}. A peak red shift of 2.9 cm^{-1} from the crystalline TO phonon peak of single crystalline silicon bulk (520.3 cm^{-1}) was observed. This means that there was a tensile stress of 5.6×10^8 Pa in the crystallized films on the quartz glass substrate.[22] These results suggest that the bonding between the silicon and substrate surface was maintained and the atoms near the film-substrate interface moved negligibly so that the stress between Si/substrate was not completely released.

4. Summary

We demonstrated the crystalline grain growth in the lateral direction using the electrical current induced joule heating with tapered electrodes. When the 5-ns-pulsed laser was irradiated to 60-nm-thick silicon strips with voltage application to the silicon strips as well as capacitance, the silicon strips melted and the melting continued for 17 μs in the case of applying a voltage of 90 V and capacitor of 0.33 μF. The tapered shape of the electrode allowed spatial distribution of joule heating intensity: high intensity at the shorter side and a low intensity at the longer side. We calculated the temperature change of the silicon strip during joule heating using the two-dimensional numerical analysis program. The solidification of silicon was initiated 4.5 μs after 5-ns-pulsed laser irradiation. The solid/liquid interface moved towards the edge of the shorter side in the lateral direction. The solidification velocity was estimated to be 1.2–2.0 m/s. The cooling rate decreased from 1.7×10^8 to 6.1×10^7 K/s during the process of solidification. Transmission electron microscopy revealed that large crystalline grains ranging from 4 μm to 8 μm in the size were formed in the thin silicon films. The solidification in the lateral direction resulted in the formation of large crystalline grains. The surface of the silicon film was shown to be very flat by stylus step measurement. Raman scattering measurements demonstrated that the crystallized films had a tensile stress of 5.6×10^8 Pa on quartz substrates.

Acknowledgments

The authors thank Mr. K. Fukuda, Mr. K. Ohkita, Mr. T. Watanabe, Professors T. Saitoh and T. Mohri for their support. This research was partly supported by the Foundation for Promotion of Material Science and Technology of Japan (MST Foundation).

1) T. Sameshima, S. Usui and M. Sekiya: IEEE Electron Device Lett. **7** (1986) 276.
2) K. Sera, F. Okumura, H. Uchida, S. Itoh, S. Kaneko and K. Hotta: IEEE Trans. Electron Devices **36** (1989) 2868.
3) T. Serikawa, S. Shirai, A. Okamoto and S. Suyama: Jpn. J. Appl. Phys. **28** (1989) L1871.
4) A. Kohno, T. Sameshima, N. Sano, M. Sekiya and M. Hara: IEEE Trans. Electron Devices **42** (1995) 251.
5) A. Matsuda: J. Non-Cryst. Solids **59–60** (1983) 767.
6) Y. Chida, M. Kondo and A. Matsuda: J. Non-Cryst. Solids **198–200** (1996) 1121.
7) K. Nakahata, A. Miida, T. Kamiya, Y. Maeda, C. M. Fortmann and I. Shimizu: Jpn. J. Appl. Phys. **37** (1998) L1026.
8) H. Matsumura: Jpn. J. Appl. Phys. **37** (1998) 3175.
9) K. H. Lee, J. K. Park and J. Jang: IEEE Trans. Electron Devices **45** (1998) 2548.
10) H. Kuriyama *et al*: Jpn. J. Appl. Phys. **31** (1992) 4550.
11) T. Sameshima: Jpn. J. Appl. Phys. **32** (1993) L1485.
12) J. S. Im and H. J. Kim: Appl. Phys. Lett. **64** (1994) 2303.
13) R. Ishihara, W.-C. Yeh, T. Hattori and M. Matsumura: Jpn. J. Appl. Phys. **34** (1995) 1759.
14) K. Okamoto and H. Suzunaga: Appl. Phys. Lett. **42** (1983) 809.
15) T. Sameshima, K. Ozaki and N. Andoh: Appl. Phys. A **71** (2000) 1.
16) N. Andoh, K. Ozaki, H. Takahashi and T. Sameshima: Proc. Workshop on Active Matrix Liquid Crystal Displays, Tokyo, Japan 2000, p. 261.
17) T. Sameshima and K. Ozaki: Jpn. J. Appl. Phys. **39** (2000) L651.
18) T. Sameshima, N. Andoh and H. Takahashi: J. Appl. Phys. **89** (2001) 5362.
19) R. F. Wood and G. E. Giles: Phys. Rev. B **23** (1981) 2923.
20) A. Goldsmith, T. E. Waterman and H. J. Hirschorn: *Handbook of Thermophysical Properties of Solid Materials* (Pergamon Press, New York, 1961) Vols. 1 and 3.
21) V. M. Clazov, S. N. Chizhenvskaya and N. N. Glagoleva: *Liquid Semiconductors* (Plemum Press, New York, 1969) p. 60.
22) B. A. Weinstein and G. J. Piennarini: Phys. Rev. B **12** (1975) 1172.