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Rapid crystallization of silicon films using pulsed current-induced joule heating

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Abstract

Crystallization of silicon films formed on glass substrates was achieved by rapid-joule heating of Cr strips adjacently formed via 200-nm-thick SiO_2 intermediate layers. 3-μs-pulsed voltages applied to the Cr strips caused a high joule heating intensity about 1×10^6 W/cm^2. Transmission electron microscopy measurements confirmed a crystalline grain size of 50–100 nm. 1-μm-long crystalline grain growth was observed just beneath of the edge of Cr strips. The activation of phosphorus atoms according to crystallization was also achieved.

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1. Introduction

Polycrystalline silicon films have been applied to many devices such as thin film transistors (TFTs) and solar cells [1–6]. Many technologies have been reported for formation of polycrystalline silicon films at low processing temperatures such as pulsed laser crystallization, plasma enhanced chemical vapor deposition (PECVD), catalytic chemical vapor deposition and metal-induced crystallization [1–10]. This paper reports a simple rapid heating method using electrical-current-induced joule heating of metal films for crystallization of silicon films [11]. Properties of rapid-joule heating followed by silicon melting are discussed with transient conductance measurements and heat flow simulation. We also discuss crystallographic and electrical properties of silicon films crystallized by the present rapid heating method. Crystalline grain distribution is reported by transmission electron microscopy. Activation of phosphorus atoms doped in the silicon films is also discussed.

2. Experimental

Fig. 1(a) shows schematic apparatus of the present heating method. 50-nm-thick amorphous silicon films were formed on quartz glass substrates were formed by low-pressure chemical vapor deposition (LPCVD). For some samples, 7×10^{17} cm^{-3} phosphorus doping was carried out by ion implantation. 8×10^{20} cm^{-3}-phosphorus-doped 50-nm-thick amorphous silicon film were also formed by plasma enhanced chemical vapor deposition (PECVD). 200-nm-thick SiO_2 films

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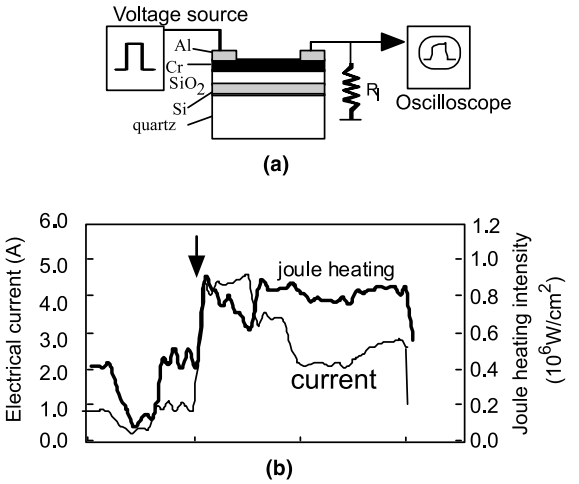

Fig. 1. Schematic apparatus of the present electrical-current-induced joule heating method and the cross section of the layered structure of samples. 3-μs-pulsed voltages was applied to the 100-nm-thick Cr strip with a length of 250 μm and a width of 50 μm, which was formed on 200-nm-thick SiO_2/50 -nm-thick silicon layers (a) and electrical current and joule heating intensity generated at the Cr strips as functions time with 80 V applied to the Cr strips.

were formed on the silicon film by sputtering. 100-nm-thick Cr films were subsequently formed on the SiO_2 films. Cr strips with a length of 250 μm and a width of 50 μm were defined by etching. Al electrodes were also formed at the edge regions of the Cr strips to apply electrical voltages to the Cr strips. 3-μs-pulsed voltages were applied to the samples. The electrical current was measured as a voltage at the 2.5-Ω-load resistance connected between sample and ground using a digital oscilloscope. We used transmission electron microscope (TEM) to observe the distribution of crystalline grains. The electrical conductivity was measured for phosphorus-doped silicon films.

3. Results

Fig. 1(b) shows changes in the electrical current flow in the Cr strips and the intensity of electrical-current-induced joule heating at 80 V. The electrical current decreased for the initial 0.6 μs. Afterwards, a rapid increase in the electrical current was observed at the time pointed by the arrows in Fig. 1(b). The joule heating intensity per unit area $W(t)$ was estimated from the electrical current was measured as a voltage V_l at the load resistance R_l connected between sample and ground using a digital oscilloscope, as shown in Fig. 1(a). $W(t)$ was *given* as $(V_0 - V_l(1 + R_s/R_l))V_l(R_lS)^{-1}$, where V_0 is the applied voltage, R_s is the series resistance of the circuit and S is the area of the Cr strips. A peak joule-heating intensity 9×10^5 W/cm^2 was achieved.

We estimated the temperature change of silicon caused by time-dependent joule heating shown in Fig. 1(b) using a numerical analysis program constructed with a system of heat flow equations for multiple layered structure with different materials [12,13]. The temperature of the silicon thin films was determined by the heat balance between heat supply from the joule heating intensity generated at Cr top layer as shown in Fig. 1(b) and heat dissipation into glass substrates. We assumed that silicon was melted at 1685 K for every heating case and the temperature was kept at the melting point until the latent heat energy (1810 J/g) was given to the silicon layer. Fig. 2 shows temperature change at silicon films 200 nm apart from the Cr strips during and after the electrical-current-induced joule heating of the Cr strips. The calculation indicated that voltage application above 70 V heated silicon to the melting point. The duration at the melting point increased from 0.8 to

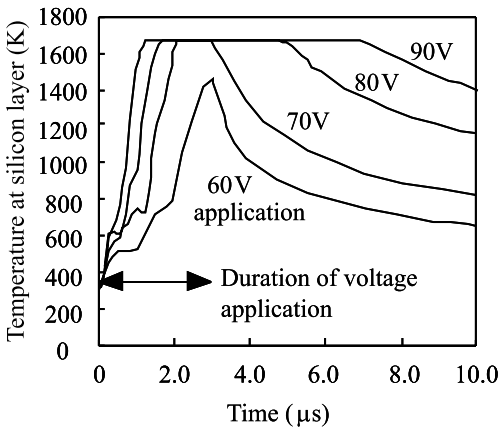

Fig. 2. Temperature change at the 50-nm-thick silicon films from initiation of 3-μs-pulsed voltage application estimated by numerical heat flow analysis with an assumption of 1685-K-melting point of silicon.

4.6 μs as the voltage increased from 70 to 90 V. Temperature at the melting point continued after termination of joule heating in the cases of voltage application at 80 and 90 V.

Fig. 3(a) shows a photograph of the bright field image of TEM plane view for undoped silicon films crystallized by 80 V application. The silicon region underlying the Cr strips was completely crystallized. Fine crystalline grains were formed. TEM image showed that the crystalline grains size ranged from 50 to 100 nm as shown in Fig. 3(b). Formation of 1-μm-large crystalline grains was also observed at the region underlying the edge of the Cr strips, as shown in Fig. 3(a).

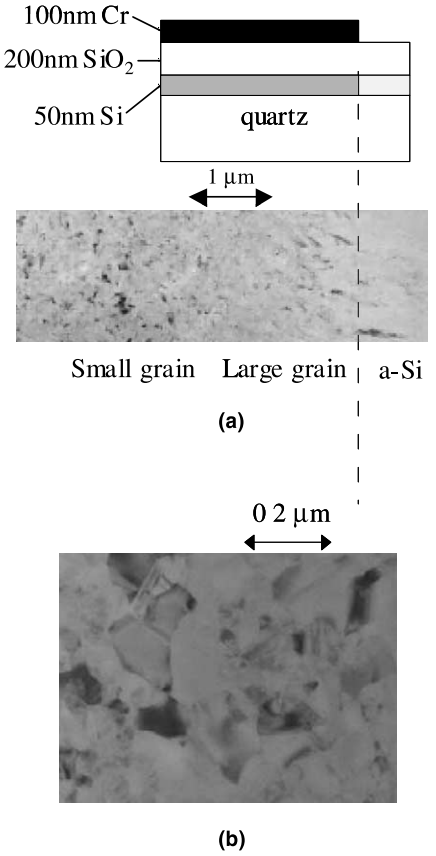

Fig. 3. Photograph of the bright field image of TEM plane views with magnifications of 5000 (a) and 20 000 (b) for the 50-nm-thick silicon films crystallized by the present method at 80 V. The schematic cross section of the samples were also illustrated.

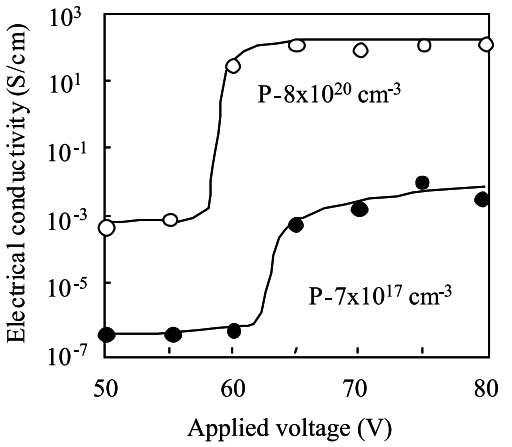

Fig. 4. Electrical conductivity as a function of the voltage applied to the Cr strips for 7×10^{17} and 8×10^{20} -cm^{-3} phosphorus-doped silicon films.

Fig. 4 shows the electrical conductivity as a function of the applied voltage for the 7×10^{17} and 8×10^{20}-cm^{-3}-phosphorus-doped silicon films. For the 7×10^{17} -cm^{-3}-phosphorus-doped silicon films, the electrical conductivity was very low 10^{-7}–10^{-6} S/cm for joule heating with voltage application between 50 and 60 V. On the other hand, the increase in the electrical conductivity occurred at a joule heating energy density of 1.2 J/cm^2 with 65 V application. The electrical conductivity increased to 4×10^{-3} S/cm as the voltage increased from 65 to 75 V. For the 8×10^{20} -cm^{-3}-phosphorus-doped silicon films, the electrical conductivity increased to 120 S/cm when the silicon films were annealed by the present heat treatment at a voltage above 65 V.

4. Discussion

The present joule heating method using is constructed by a simple electrical circuit. Electrical current caused μs-order high intensity of joule heating. When 80 V was applied to the Cr strip, a high electrical current ~1 A was observed at the initial stage. Afterwards, it decreased with time because of the resistivity increase of Cr due to the electrical-current-induced joule self heating. Increase in the electrical current was observed from 0.6 μs. This increase results from decrease of the

resistivity probably associated with melting of Cr strips caused by heating to high temperature above the melting point of Cr, 2165 K. The resistivity of molten Cr was estimated about 8×10^{-6} Ω cm. The high electrical current caused the high joule heating intensity, as shown in Fig. 1(b). A peak joule-heating intensity 9×10^5 W/cm^2 was achieved when the Cr strip was melted and its resistance decreased.

Temperature change of the silicon layer caused by joule heating at top Cr layer via heat diffusion through the SiO_2 intermediate layer was estimated using numerical calculation program. Because the present heating continued 3 μs, heat diffused about 1.5-μm deep from the surface during heating. Heat diffusivity of quartz therefore determined temperature of silicon layers. The calculation indicated that voltage application above 70 V heated silicon to the melting point. The duration at the melting point increased from 0.8 to 4.6 μs as the voltage increase from 70 to 90 V. Temperature at the melting point continued after termination of joule heating in the cases of voltage application at 80 and 90 V. The heat flow calculation suggests that there is the possibility of rapid melting followed by crystallization of silicon films.

Crystallization of silicon films was confirmed by TEM observation. The crystalline grains size ranged from 50 to 100 nm as shown in Fig. 3(b). The fine grains were formed close to each other and no substantial disordered region was observed at the grain boundary. Heat flow calculation and TEM observation indicate that the silicon films were melted by the present heat treatment and then solidified to crystalline states after termination of the joule heating. Interesting result was the formation of 1-μm-large crystalline grains at the region underlying the edge of the Cr strips, as shown in Fig. 3(a). The large crystalline grains were probably formed laterally according to temperature distribution formed in the lateral direction associated with heat dissipation from the edge of Cr strips during the joule heating. This TEM result indicates the possibility of formation of large crystalline grains by the present crystallization method.

Dopant activation was investigated for doped silicon films. The electrical conductivity increased to 4×10^{-3} and 120 S/cm for the 7×10^{17} and 8×10^{20}-cm^{-3}-phosphorus-doped silicon films, respectively. The increase in the electrical conductivity caused by the electrical-current-induced joule heating means that the phosphorus atoms were activated according to the crystallization of silicon films and the electron carriers were generated by the heating. The increase in the electrical conductivity occurred at a joule heating energy density of 1.2 J/cm^2 with 65 V application. That energy density was lower than that of 1.9 J/cm^2 for crystallization of undoped silicon films. We interpret that ion implantation of phosphorus atoms increases disordered states of silicon bonding network and reduced the melting threshold of silicon films so that the doped silicon was crystallized and dopant atoms were activated at the low heating energy density. Activation of dopant atoms as well as crystallization of silicon films will be useful for fabrication of TFTs.

5. Summary

We reported a simple crystallization method for silicon films by the electrical-current-induced joule heating at Cr strips formed on 50-nm-thick silicon films via 200-nm-thick SiO_2 intermediate layers. 3-μs-pulsed voltages were applied to Cr strips with a length of 250 μm and a width of 50 μm. Numerical heat flow analysis suggested that the silicon films were heated to the melting point of silicon by the electrical-current-induced joule heating generated above 1.4 J/cm^2. Transmission electron microscopy measurements confirmed a crystalline grain size of 50–100 nm. 1-μm-long crystalline grain growth was also observed in the region just beneath the edge of Cr strips. The electrical conductivity increased to 120 S/cm for 8×10^{20}-cm^{-3}-phosphorus-doped silicon films. These mean the activation of phosphorus atoms according to crystallization. The present crystallization and activation method will be useful for fabrication of electric devices such as TFTs.

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