# Large crystalline grain growth using current-induced Joule heating

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**Abstract.** Electrical-current-induced Joule heating was applied to crystallization of 60-nm-thick amorphous silicon films formed on glass substrates. 3- $\mu$ s-pulsed voltages were applied to silicon films connected with a capacitance in parallel. Coincident irradiation with 28-ns-pulsed excimer laser melted films partially and reduced its resistance. Complete melting for 12  $\mu$ s and a low cooling rate at  $1.1 \times 10^8$  K/s were achieved by Joule heating from electrical energy accumulated in the capacitance at  $0.22 \,\mu$ F. For  $7.4 \times 10^{17} \,\text{cm}^{-3}$  phosphorus-doped films, analysis of temperature change in the electrical conductivity gave that the density of defect states localized at grain boundaries was  $1.5 \times 10^{12} \,\text{cm}^{-2}$ . Formation of 3.5- $\mu$ m-long crystalline grains was observed by transmission electron micrograph. Preferential crystalline orientation was (110).

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Polycrystalline silicon films have been applied to many devices such as thin film transistors (TFTs) and solar cells [1–6]. Formation of polycrystalline silicon films at low cost has been demanded in recent years for fabrication of large-area devices. Many technologies have been reported for formation of polycrystalline silicon films at low processing temperatures [1-10]. Pulsed laser crystallization method has an advantage for formation high-quality polycrystalline silicon films via rapid melting followed by solidification. That method has been therefore applied to fabrication of poly-Si TFTs and its electronic circuits. However, it is important to fabricate large crystalline grains with a low density of defect states especially for solar cell application. Although several methods have been reported for formation of large crystalline grains using the pulsed laser crystallization method [11-13], it is not easy to control solidification properties of crystallization velocity, cooling rate, solidification duration because the laser pulse is too short to control the solidification temperature during the crystallization process.

In this paper, we propose a crystallization method with pulsed electrical current-induced heating of silicon films in order to fabricate large crystalline grains. We report that silicon thin films are melted for a long time and its melt duration is easily controlled by electrical current intensity. Large grain growth of  $3.5 \,\mu\text{m}$  is demonstrated. Electrical properties of the crystalline grains and grain boundaries are analyzed and a low density of defect states is demonstrated. Photoconductivity of the crystalline films is also reported.

## 1 Experimental

Undoped amorphous silicon films 60 nm thick were formed by low-pressure CVD methods on quartz glass substrates. Some silicon films were doped with phosphorus atoms at  $7.4 \times 10^{17}$  cm<sup>-3</sup> using the ion implantation method. Their undoped and lightly-doped silicon strips with a width of 50 µm were defined by lithography and etching methods. Al electrodes with a gap of  $250 \,\mu m$  were formed on the silicon strips. The samples were placed in a vacuum chamber and connected by metal probes to Al electrodes to apply electrical voltages to the silicon films. A voltage source generating pulsed voltages with a pulse width of  $3 \mu s$  was used to heat the silicon films. The pulsed voltages were applied to the samples via simple electrical circuits with a series resistance, resistance of silicon and load resistance, as shown by the inset in Fig. 1. In coincidence with the voltage pulse, samples were irradiated with 28-ns pulsed XeCl excimer laser to melt silicon films partially during the voltage application. Because of an experimental system delay, laser pulses were shined to samples about 2.1 µs after the initiation of the pulsed voltage application. Although silicon films have a high resistivity in solid phase at room temperature because of a low carrier density, the resistance of silicon markedly decreases when silicon is melted because liquid silicon has the metallic phase. Laserinduced melting during voltage application therefore causes a high Joule heating per unit area induced by electrical current,  $I^2 R_{\rm Si}/S$ , where S is the area (width  $\times$  length) of silicon films. The electrical current was measured as a voltage at a load resistance connected between sample and ground using a high-speed digital oscilloscope. We used transmission electron micrographs (TEM) to observe distribution of crystalline grains and their crystalline orientation. Stylus step measurements were also used to investigate film thickness distribution after crystallization.

The temperature change in the electrical conductivity was measured to analyze electrical properties of grain bound-



**Fig. 1.** Changes in the electrical current flowing at silicon. The samples were heated only with laser irradiation at 400 mJ/cm<sup>2</sup> as well as with laser irradiation at 400 mJ/cm<sup>2</sup> during application of a 3- $\mu$ s pulsed voltage at 110 V. Equivalent circuit is shown by *inset*. Series resistance  $R_s$  and load resistance  $R_1$  were 4.0 and 4.8  $\Omega$ . 60-nm-thick silicon strips with a width of 50  $\mu$ m and a length 250  $\mu$ m were formed on quartz glass substrates

aries for the phosphorus doping case. Photoconductivity was measured for undoped silicon films under the illumination of 1700 K black-body radiation at 40 mW/cm<sup>2</sup>. For the photoresponse measurements, surface passivation was conducted by high-pressure H<sub>2</sub>O-vapor annealing [14, 15] in order to reduce the carrier recombination velocity at the sample surface after crystallization. 200-nm-thick  $SiO_x$  films were deposited at room temperature on the silicon surface by thermal evaporation in vacuum under a base pressure of  $4 \times 10^{-4}$  Pa using a turbo-molecular pump. The samples  $(SiO_x/Si/quartz)$  were placed into a pressure-proof stainless steel chamber using a metal seal. Pure water was also put into the chamber. The chamber was then placed on a heater plate to heat samples at 270 °C for 3 h. The H<sub>2</sub>O evaporated during heating and the gas pressure increased to  $1.3 \times 10^6$  Pa. During treatment,  $SiO_x$  is oxidized by high-pressure H<sub>2</sub>O vapor and changed into SiO<sub>2</sub>. Through the treatment, the surface recombination velocity is reduced to 20 cm/s for crystalline silicon substrate.

### 2 Results

Figure 1 shows changes in the electrical current flowing at silicon films with time. The samples were heated only with laser irradiation at 400 mJ/cm<sup>2</sup> as well as with laser irradiation at 400 mJ/cm<sup>2</sup> during application of a pulsed voltage at 110 V. A small current peak was observed for a very short period  $\approx 50$  ns for simple laser irradiation at 400 mJ/cm<sup>2</sup> according to laser-induced rapid and short melting of silicon films. On the other hand, a long melting was observed when silicon was applied by a pulsed voltage at 110 V in coincidence with laser irradiation, as shown in Fig. 1. The high electrical current at  $\approx 3$  A almost leveled off until the termination of the pulsed voltage. This means that the silicon films were completely melted and the resistance was limited by the resistivity of liquid silicon.

In order to melt silicon films for a longer time than the voltage pulse duration and control electrical current precisely, a simple circuit was developed with a capacitance connected to silicon films in parallel, as shown by an equivalent circuit in Fig. 2a. The electrical current flowing in the silicon films is controlled by a value of the capacitance. If the resistances and the capacitance are constant with time in the equivalent circuit, the electrical current at silicon films at a time t is given by simple formula as

$$t \le T:$$

$$I(t) = \frac{V_0}{R_1 + R_{\text{Si}}} \left( 1 - \frac{R_{\text{s}}}{R_{\text{s}} + R_1 + R_{\text{Si}}} \right)$$

$$\times \left( 1 - \exp\left(-\frac{R_{\text{s}} + R_1 + R_{\text{Si}}}{(R_1 + R_{\text{Si}}) R_{\text{s}}C}t\right) \right),$$

$$t > T:$$

$$I(t) = I(T) \exp\left(-\frac{t-T}{C(R_{\rm l}+R_{\rm Si})}\right),\tag{1}$$



**Fig. 2a,b.** Equivalent circuit with a cpapacitance *C* in parallel with silicon films (**a**) and electrical current obtained experimentally with a capacitance of  $0.22 \,\mu\text{F}$  as a function of time and calculated current using (1) with an assumption that silicon films were completely melted and had a constant and minimum resistance (**b**). A voltage pulse at 125 V was used to obtain almost the same maximum current for the no capacitance case as shown in Fig. 1. An *arrow* shows the point at which the experimental electrical current started decreasing more rapidly compared with the calculated current. The arrow means the solidification initiation points

where  $R_s$ ,  $R_{Si}$ ,  $R_l$  are the series resistance, the resistance of silicon films, and the load resistance, C is the capacitance,  $V_0$  is the output voltage at voltage source and T is the pulse duration of voltage source.

Figure 2b shows the electrical current obtained experimentally with a capacitance of  $0.22 \,\mu\text{F}$  as a function of time and also shows calculated current using Eq. (1) with an assumption that silicon films were completely melted and had a constant and minimum resistance. The resistance of silicon was obtained by fitting calculated current to experimental current at maximum. Laser irradiation initiated an increase of the electrical current. The electrical current reached maximum at the termination of voltage pulses at 3 µs. After that, the electrical current was still observed. Both of the experimental and calculated electrical currents decreased with time for a while keeping their current same after termination of the voltage pulses. This means that the resistance of silicon films did not change because the current-induced Joule heating kept silicon in the melting state for a long time. However, the experimental electrical current started decreasing more rapidly at a point indicated by an arrow in Fig. 2b compared with that given by Eq. (1) with a constant  $R_{Si}$ . This reduction of the electrical current means the increase of the resistance of silicon films. It indicates the solidification initiation point. The solidification initiated at 7.8 µs after termination of the voltage pulses for the capacitance increased of 0.22 µF, as shown in Fig. 2. We also obtained the solidification duration determined as the time between the solidification initiation point and the point at which the electrical current reduced to zero. It was  $4.5 \,\mu s$ . This means that the present current-induced Joule heating makes it possible to control the melt duration, the cooling rate of silicon film, and the solidification duration, which are important parameters for crystallization of silicon films.

We estimated the cooling rate with numerical analysis of heat diffusion into the glass substrate under the condition of time-dependent Joule heating. We assumed that there was no substantial super cooling and silicon was solidified at the melting point at 1412 °C for every heating case. A numerical analysis of temperature change was conducted using the heat flow equation [16] as

$$\delta T/\delta t = Q(t)/c\rho + \delta/\delta z (D\delta T/\delta z), \qquad (2)$$

where T, Q, z are temperature, heating energy intensity, and depth, respectively, and c,  $\rho$ , D are specific heat, density, heat diffusion coefficient for silicon and glass [16, 17]. Because the electrical current flowing in silicon films is obtained by measuring voltage at the load resistance, the intensity of the electrical current-induced Joule heating at silicon films per unit volume is simply described as

$$Q(t) = \frac{R_{\rm Si}I(t)^2}{V} = \left(\frac{V(t)}{I_{\rm measured}(t)} - R_{\rm I}\right)\frac{I_{\rm measured}(t)^2}{V},\qquad(3)$$

where  $I_{\text{measured}}$  is the electrical current obtained experimentally, as shown in Figs. 1 and 2, V(t) is the calculated voltage applied at the capacitance, V is the volume of the silicon strips. The heating intensity given by Eq. (3) was used for the calculation of cooling rate at silicon films until the solidification initiation point under the assumption that silicon solidified at the melting point at the time experimentally obtained, as shown in Fig. 2b. The cooling rate at the solidification point was estimated as about  $1.1 \times 10^8$  K/s for crystallization with a capacitance of  $0.22 \,\mu$ F. On the other hand, the cooling rate was  $6.5 \times 10^8$  K/s for crystallization with no capacitance. The present current-induced Joule heating reduced the cooling rate accompanied by an increase of melt duration. A high capacitance reduced the cooling rate to  $\approx 1 \times 10^8$  K/s at the solidification point in the present condition. In contrast, simple pulsed laser heating results in a very high cooling rate  $\approx 10^{10}$  K/s because of the very short melt duration < 100 ns [18].

Transmission electron micrographs (TEM) was used for observation of the distribution of crystalline grains. Figure 3a shows a photograph of the bright-field image at the edge region of silicon strips crystallized by the present method with a capacitance of  $0.22 \,\mu\text{F}$ . Crystalline grains about  $3.5 \,\mu\text{m}$ long were formed from the edge. The width of the grains was rather narrow at about 0.5 µm. Crystalline grains were closely formed next to each other and there is no substantial disordered region among them. Figure 3b shows a diffraction pattern of a crystalline grain indicated by (A) in Fig. 3a. The diffraction pattern shows that the crystalline grain had a single-crystalline domain with a crystalline orientation of (110) normal direction to the substrate. TEM observation with carefully changing of the incident angle of the electron beam to the samples revealed that the preferential crystalline orientation of (110) distributed within plus or minus 1° among crystalline grains shown in Fig. 3a.

Large grain growth at edge regions indicates that crystallization probably initiated at the edge of the silicon strips and it proceeded inside. The solidification velocity was roughly estimated from the average crystallization duration 4.5 µs and the average grain size 3.5 µm obtained by measurements of transient electrical current and TEM observation as shown in Figs. 2 and 3. It was about 0.8 m/s (= 3.5/4.5). Interesting is that the crystallization velocity for the present method is almost the same as that for simple pulsed laser crystallization of silicon thin films formed on glass substrate [19], although the melt duration and the cooling rate were very different between those methods. Figure 4 shows the film thickness distribution around the edge regions of silicon strips measured by a stylus step equipment. Although the average film thickness was 60 nm, increase of the thickness to 80 nm was observed at the edge region for crystallization with a capacitance of  $0.22 \,\mu\text{F}$ . This increase of the thickness occurred associated with large crystalline grain growth from the edge. The silicon films undergo a change of shape into a globular shape due to surface tension during melting. The change in thickness was small compared with the length of the lateral grain growth,  $3.5 \,\mu\text{m}$ . Formation of thin and large crystalline grains was achieved with the present current-induced Joule heating method.

Figure 5 shows the electrical conductivity as a reciprocal function of absolute temperature for  $7.4 \times 10^{17}$  cm<sup>-3</sup> phosphorus-doped silicon films crystallized by the electricalcurrent-induced Joule heating with a capacitance of  $0.22 \,\mu\text{F}$  and no capacitance as well as for simple laser crystallization at 400 mJ/cm<sup>2</sup>. Al electrodes with a narrow gap of 4  $\mu$ m were formed after crystallization at edge regions of silicon strips as shown by the inset in Fig. 5. For simple laser crystallization at 400 mJ/cm<sup>2</sup>, the electrical conductivity was very low at room temperature and it rapidly increased with an activa-







(b)

**Fig. 3a,b.** Photograph of the bright-field image at the edge region of silicon strips crystallized by the electrical current-induced Joule heating method with a capacitance of  $0.22 \,\mu\text{F}$  and a pulsed voltage at  $125 \,\text{V}$  (**a**), and diffraction pattern at a crystalline grain indicated by (A) in the photograph (**a**) (**b**)

tion energy of 0.54 eV as the temperature increased. On the other hand, high electrical conductivities were observed for the current-induced Joule heating cases and its activation energy decreased, as shown in Fig. 5. For crystallization in the 0.22- $\mu$ F capacitance case, the electrical conductivity and the activation energy were obtained as 3.5 S/cm and 0.042 eV, respectively.

We analyzed changes in the electrical conductivity of polycrystalline films using a statistical thermodynamical analysis program [20-22]. We introduced a Gaussian-type energy distribution of density of defect states in the band gap at grain boundaries. Phosphorus dopant atoms were assumed to be distributed uniformly in silicon films. Electron



Fig. 4a,b. Film thickness distribution around the edge regions of silicon strips measured by a stylus step equipment for crystallization with no capacitance (a) and a capacitance of  $0.22 \,\mu\text{F}$  (b)



**Fig. 5.** Electrical conductivity measured (*dotted curves*) and calculated (*solid curves*) as a reciprocal function of absolute temperature for  $7.4 \times 10^{17}$  cm<sup>-3</sup> phosphorus-doped silicon films crystallized by the electrical current-induced Joule heating with a capacitance at  $0.22 \,\mu\text{F}$  and no capacitance as well as for simple laser crystallization at 400 mJ/cm<sup>2</sup>. Inset presents image of Al electrodes with a narrow gap of 4  $\mu$ m formed at the edge region of silicon strips after crystallization

carriers are generated from the phosphorus dopant atoms via their ionization, whose probability is determined with the Fermi-Dirac statistical distribution function. Free carriers are trapped by the localized defect states and the defects are charged negatively. The Fermi energy level is determined by the statistical thermodynamical conditions keeping the charge neutrality among the densities of ionized dopant atoms  $(N_d)$ , defect states charged negatively with electron carriers  $(X_d)$  and free carriers (n),  $N_d = n + X_d$ , in the whole region including crystalline grains and grain boundaries. However, the density of ionized donors is larger than that of free electrons in crystalline grains because some electrons produced from doped phosphorus atoms are trapped at grain boundaries. This space-charge effect in crystalline grains causes the band bending and results in the potential barrier at grain boundaries. We also introduced scattering effects due to dopant ions, lattice vibration, and disordered states at grain boundaries, which reduces the carrier mobility [23, 24].

Agreement between temperature dependencies of calculated and experimental conductivities revealed that planes of grain boundaries had a high defect density at  $3.8 \times 10^{12}$  cm<sup>-2</sup>

for the case of simple laser crystallization at  $400 \text{ mJ/cm}^2$ . In this estimation, the average grain size was 45 nm determined by TEM observation. For the crystallization of silicon films by electrical current-induced Joule heating, we did not determine distribution of crystalline grains and the number of grain boundaries in 4-µm-long electrodes, we hypothesized that there was a single grain boundary between electrodes. We introduced a numerical factor (< 1) to obtain the effective width of the electrode for fitting the calculated electrical conductivity to the experimental one because the electrical current must flow along a path, which has a lowest number of grain boundaries or has grain boundaries with the lowest potential barrier. For crystallization with no capacitance, best agreement between calculated and experimental temperature change of the electrical conductivity gave the density of defect states per unit area at grain boundaries as  $1.5 \times 10^{12} \text{ cm}^{-2}$ , which was much lower than that of silicon films by laser crystallization. The potential barrier height at grain boundaries was 0.11 eV at room temperature. On the other hand, calculation of temperature change of the electrical conductivity assumed with no defect states gave a good agreement with the experimental result for crystallization with  $0.22 \,\mu\text{F}$ , as shown in Fig. 5. The electrical conductivity gradually increased with an activation energy of 0.042 eV as temperature increased only because the ionization probability of dopant atoms and the density of thermionic carrier increased. Single-domain crystalline regions were probably formed in the 4-µm-long electrodes via crystallization with a low cooling rate at  $\approx 1.1 \times 10^8$  K/s and long melt duration of 12 µs.

The photoconductivity was investigated for undoped silicon films to look for a possibility of application to photovoltaic devices. In the present experimental condition, the photoconductivity was  $1.7 \times 10^{-3}$  S/cm and  $1.2 \times 10^{-2}$  S/cm for silicon films crystallized by laser irradiation at 400 mJ/cm<sup>2</sup> and electrical current-induced Joule heating with a capacitance of 0.22  $\mu$ F, respectively. When silicon films are thin enough and photoresponse is proportional to the light intensity, the photoconductivity  $\sigma_{ph}$  at a wavelength  $\lambda$  is:

$$\sigma_{\rm ph} = \eta \mu \tau e \alpha (1-R) P \,,$$

where  $\eta$  is the generation efficiency,  $\mu$  is the carrier mobility,  $\tau$  is the average carrier life time, *e* is the elemental charge,  $\alpha$  is the absorption coefficient, R is the reflectivity, and P is the photon flux (photons  $cm^{-2} s^{-1}$ ). Narrow wandpath optical filters were used to measure photoresponse with different wavelengths. Light intensity was measured using germanium and silicon photosensors. The absorption coefficient was assumed as that of single-crystalline silicon. The reflectivity spectra were calculated with consideration of the interference effect for air/SiO<sub>2</sub>/silicon film/quartz substrate. Figure 6 shows the  $\eta\mu\tau$  product as a function of photon energy. The  $\eta\mu\tau$  product for crystallization with a capacitance  $0.22 \,\mu\text{F}$  was high at  $\approx 10^{-3} \,\text{cm}^2/\text{V}$  compared with that for simple laser crystallization at 400 mJ/cm<sup>2</sup>. The large crystalline grain formation probably increased the carrier lifetime markedly because low grain boundary density resulted in low carrier trapping probability especially for minority carriers. The high  $\eta\mu\tau$  product of thin silicon films will be interesting in applications of the present crystallization method to solar cells as well as thin-film photosensors.



**Fig. 6.** Products of generation efficiency,  $\eta$ , carrier mobility,  $\mu$ , and average carrier life time,  $\tau$ , as a function of photon energy for undoped films crystallized by the electrical current-induced Joule heating with a capacitance at 0.22  $\mu$ F and simple laser crystallization at 400 mJ/cm<sup>2</sup>

#### **3** Summary

We investigated electrical current-induced Joule heating for crystallization of silicon films. Pulsed voltages with a width of 3 µs and coincident irradiation with 28-ns-pulsed excimer laser at 400 mJ/cm<sup>2</sup> were applied to 60-nm-thick amorphous silicon films formed on glass substrates and capacitance connected in parallel. A large electrical current flowed in the silicon films and its Joule heating melted silicon films completely for a long time. The Joule heating from electrical energy accumulated at the capacitance at 0.22 µF caused the duration of complete melting and the solidification duration for 7.8 µs and 4.5 µs, respectively. Heat flow analysis gave the cooling rate at  $1.1 \times 10^8$  K/s. Transmission electron micrographs revealed that 3.5-µm-long crystalline grains were formed at edge regions. The grains were formed closely and they were lined along the silicon strip. Preferential crystalline orientation normal direction to substrate was (110). The crystalline orientation distributed within plus or minus 1° among the crystalline grains. A little thickness change from 60 nm to 80 nm was caused at the grain growth of  $3.5 \,\mu$ m. For crystallization of  $7.4 \times 10^{17}$  cm<sup>-3</sup> phosphorus-doped silicon films, the high electrical conductivity increased from 0.1 to 3.5 S/cm and it activation energy decreased from 0.17 to 0.042 eV as the capacitance increased 0 to  $0.22 \,\mu\text{F}$  when 4-µm-long electrodes were used for current measurements. The statistical thermodynamical analysis of the electrical conductivity gave the density of the defect state at grain boundary plane as about  $1.5 \times 10^{12}$  cm<sup>-2</sup> and the potential barrier height at grain boundaries was 0.11 eV for crystallization with no capacitance. For crystallization with a capacitance at  $0.22 \,\mu\text{F}$ , the temperature change in the electrical conductivity was characterized with no grain boundary. A photoconductivity at  $1.2 \times 10^{-2}$  S/cm was observed under the illumination of 1700 K black-body radiation at 40 mJ/cm<sup>2</sup>. The product of the generation efficiency, the carrier mobility and the average carrier life time was estimated  $\approx 10^{-3} \text{ cm}^2/\text{V}$ .

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