Research Activities on Nanoelectronics, Nanofabrication and Nanolithography

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Keywords: Scanning Probe Microscopy (SPM), Nanolithography Using SPM, Single-Electron Transistor (SET), Ultra-Small Tunnel Junction, Quantum Point Contact (QPC), Ferromagnetic Nanostructure, Magnetoresistance (MR), Nanofabrication Using Controlled-Electromigration Scheme (Feedback-Controlled, Field-Emission-Induced)
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1. Abstract

1.1 SHIRAKASHI GROUP -Nanoelectronics, Nanofabrication and Nanolithography-

1.2 KEYWORDS

Nanofabrication: Scanning Probe Microscopy (SPM), Atomic Force Microscopy (AFM), SPM Local Oxidation Nanolithography, SPM Scratching Nanolithography, Electron-Beam Lithography

Nanodevices: Single-Electron Transistor (SET), Ferromagnetic Single-Electron Transistor (FMSET), Ultra-Small Tunnel Junction, Ferromagnetic Tunnel Junction, Quantum Point Contact (QPC), Ferromagnetic Nanostructure

Interesting Physical Properties: Single-Electron Charging Effects, Controlled Electromigration (Voltage-Controlled, Field-Emission-Induced), Magnetoresistance (MR), Anisotropic Magnetoresistance (AMR), Tunnel Magnetoresistance (TMR), Domain Wall Magnetoresistance (DWMR), Spin Injection/Current Induced Magnetization Reversal

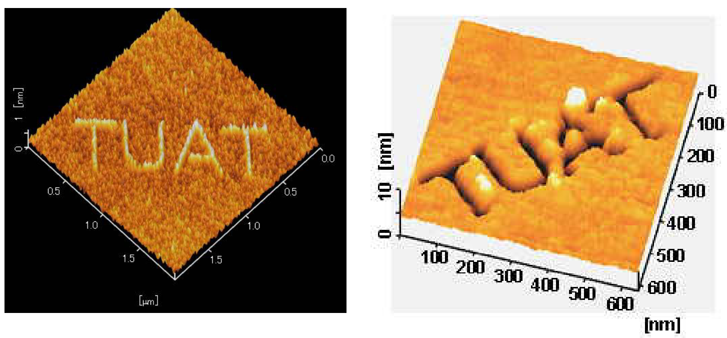
1.3 OUR GROUP'S RESEARCH

focuses on fabrication of nanodevices and measurement of their electronic and magnetic properties at low to room temperatures and includes new nanofabrication techniques, magnetoresistance properties in ferromagnetic nanodevices and transport properties of electrons through Si and metallic/ferromagnetic nanostructures such as quantum dots and nanoconstrictions.

2. Research Topics

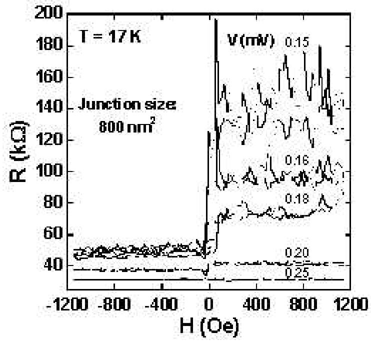
2.1 Nanolithography Using Scanning Probe Microscopy (SPM)

Scanning probe microscopy (SPM)-based lithography at the micro- and nano-scales is presented. Our method in SPM local oxidation involves two SPM tips, one having a robust blunt tip, a "micrometer tip", and the other having a sharp tip, a "nanometer tip". In tapping mode SPM local oxidation, Si oxide wires with sub-10 nm resolution were produced by precisely tuning the dynamic properties of the nanometer tip. In order to perform large-scale oxidation, SPM tip with a contact area of μm^2, which is about 10^4 times larger than that of the conventional nanometer tip, was prepared. Furthermore, we explore the possibility of performing the sub-20 nm lithography of Si surfaces using SPM scratching with a diamond-coated tip. SPM-based lithography plays an important role for bridging the gap between micro- and nano-scales.



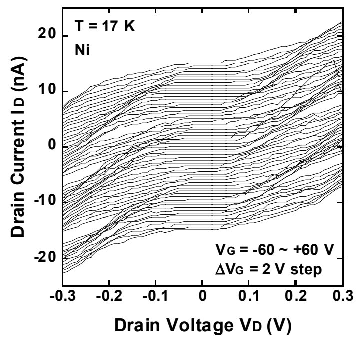
2.2 Planar-Type Ferromagnetic Tunnel Junctions

Nanometer-scale oxide wires were fabricated by local oxidation nanolithography using scanning probe microscope (SPM). This technique was applied to the fabrication of planar-type Ni/Ni oxide/Ni ferromagnetic tunnel junctions. In order to induce magnetic shape anisotropy, asymmetrical channel structure was patterned by conventional photolithography and wet etching processes. The magnetoresistance (MR) characteristics were clearly shown in the planar-type Ni/Ni oxide/Ni ferromagnetic tunnel junctions. MR ratio of above 100 % was obtained at 17 K. This result suggests that the local oxidation nanolithography using SPM is useful for the application to planar-type ferromagnetic tunnel junctions.



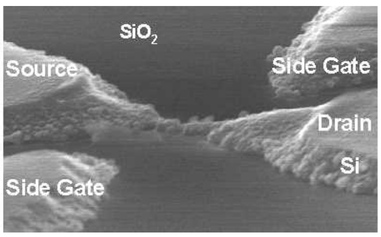
2.3 Ferromagnetic Single-Electron Transistors

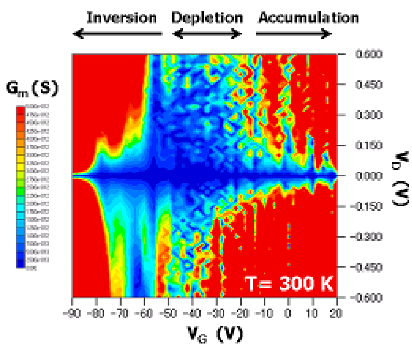
We study quantitatively the operation of ferromagnetic single-electron transistors coupled to the controlling gate potential by the gate resistance and gate capacitance in series. In this type of the device, several metastable charge states are possible within the Coulomb blockade range. The enhancement and hysteresis of tunnel magnetoresistance on the drain and gate voltages are predicted. Inelastic macroscopic quantum tunneling of charge and the existence of several charge states play an important role for the unique behavior of the tunnel magnetoresistance. This implies that RC-coupled ferromagnetic single-electron transistors have a new functionality as novel magnetoresistive nanostructure devices.



2.4 Si-Based Single-Electron Transistors

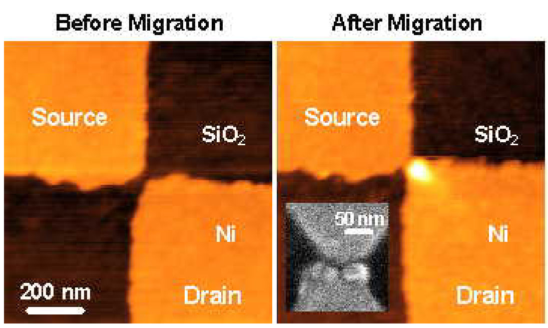
Single-electron charging effects are studied in Si-based single-electron transistors (Si-SETs) at room temperature. The SETs were first fabricated by a conventional Electron-Beam (EB) lithography method. Then the miniaturization of tunnel junctions was further performed by scanning probe microscopy (SPM)-based nanolithography techniques such as SPM local oxidation and SPM scratching. Ultra-low capacitance tunnel junctions were easily obtained by utilizing both kinds of nanofabrication processes, which realizes room temperature operation of Si-SETs.





2.5 Controlled Electromigration for Nanodevice Fabrication/Integration

We report a simple and easy technique for the fabrication of nanogaps with the separations of less than 10 nm. This technique is based on electromigration induced by field emission current. Here, we investigated the dependence of tunnel resistance on the shape of nanogap electrodes and initial gap separation. The initial nanogap electrodes having asymmetrical shape with the separation of 30-60 nm were fabricated by electron-beam lithography and lift-off process. In the nanogaps with asymmetrical shape, the tunnel resistance was controlled by the magnitude of the preset current during field-emission-induced electromigration and decreased from the order of 100 TΩ to 100 kΩ with increasing the preset current from 1 nA to 150 μA. This



tendency was quite similar to that of nanogaps with symmetrical shape. Furthermore, the tunnel resistance after the electromigration was less dependent on the initial gap separation and was completely determined by the preset current. This result suggests that it is possible to perform the control of tunnel resistance of nanogaps by field-emission-induced electromigration.

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